

COMPAL CONFIDENTIAL

**vinafix**

MODEL NAME :CDM70

PCB NO : LA-E082P

BOM P/N :

BR14 KBL-U DSC

**Kabylake U**

2016-11-07

REV : 1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

CXDP@ : XDP Component

CONN@ : Connector Component

MB PCB

Part Number	Description
DAA000CR000	PCB 1SD LA-E082P REV0 MB DSC 1

Layout Dell logo



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REV:X00  
PWB: DKJP1

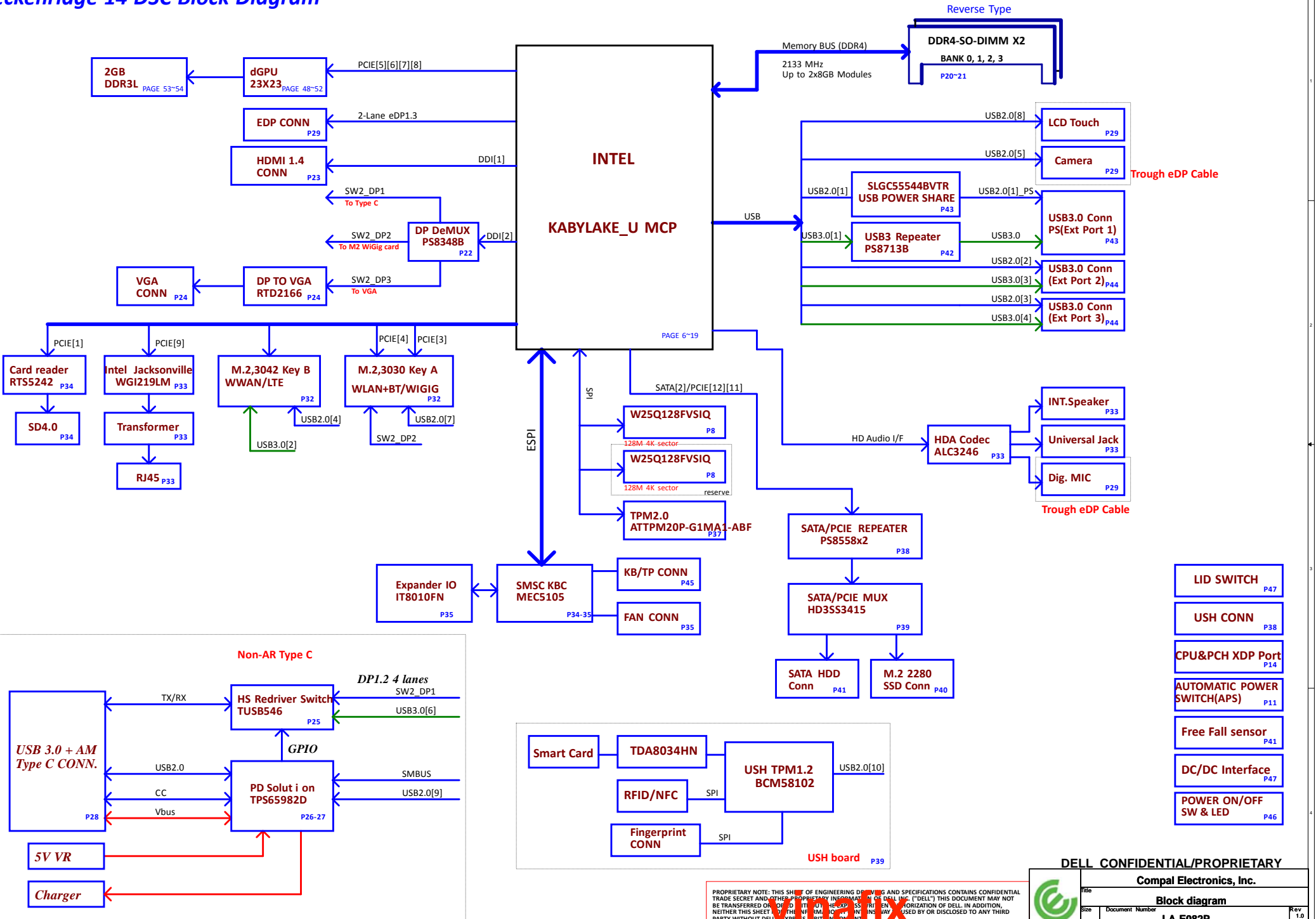
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Title		Cover Sheet	
Size	Document Number	LA-E082P	Rev 1.0
Date:	Monday, December 12, 2016	Sheet 1	of 75

Breckenridge 14 DSC Block Diagram



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POWER STATES

Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
State									
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

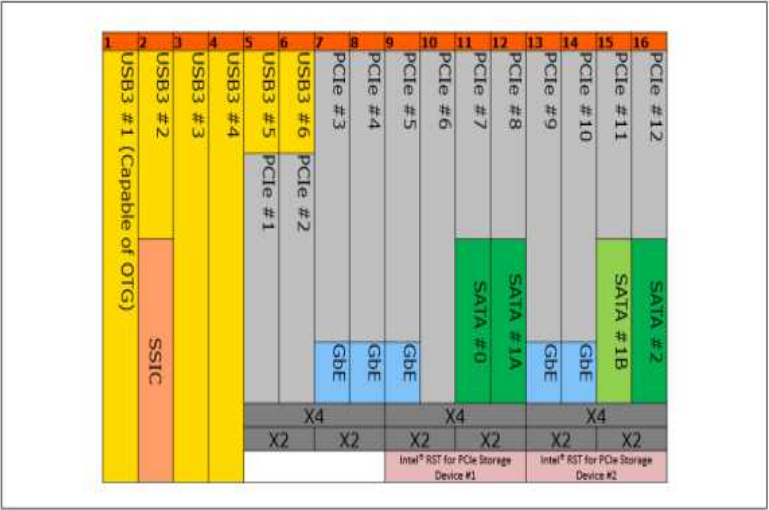
State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.5
			Add Plating		
1	Top		Copper foil	0.5oz+plating	1.6
		3.8	Prepreg	1080	2.6
2	GND		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
3	IN 1		Copper foil	1oz	1.25
		3.7	Prepreg	2116H	4.3
4	GND/PWR		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
5	IN 2		Copper foil	1oz	1.25
		3.6	Prepreg	1080H x2 orPP2116HRC	4.2
6	IN 3		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
7	GND/PWR		Copper foil	1oz	1.25
		3.8	Prepreg	2116H	4.3
8	IN 4		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
9	GND		Copper foil	1oz	1.25
		3.8	Prepreg	1080	2.6
10	Bottom		Copper foil	0.5oz+plating	1.6
			Add Plating		
			SolderMask	IT-158	0.5
Overall Thickness (1.2mm ± 10%)					47.68000 1.211072

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Lef t
USB3.0-4				JUSB3-->Rear Lef t
USB3.0-5		PCIE-1		Card Reader
USB3.0-6		PCIE-2		Type-C Port
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		M.2 3030(WIGIG)
		PCIE-6		Discrete Graphics x4
		PCIE-7	SATA-0	
		PCIE-8	SATA-1	
		PCIE-9		
		PCIE-10		LOM
				NA
		PCIE-11	SATA-1*	NA
		PCIE-12	SATA-2	M.2 2280 SSD (PCIex2 or SATA)
				SATA HDD

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2-->Lef t
3	JUSB3-->Rear Lef t
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	Type-C Port
10	USH

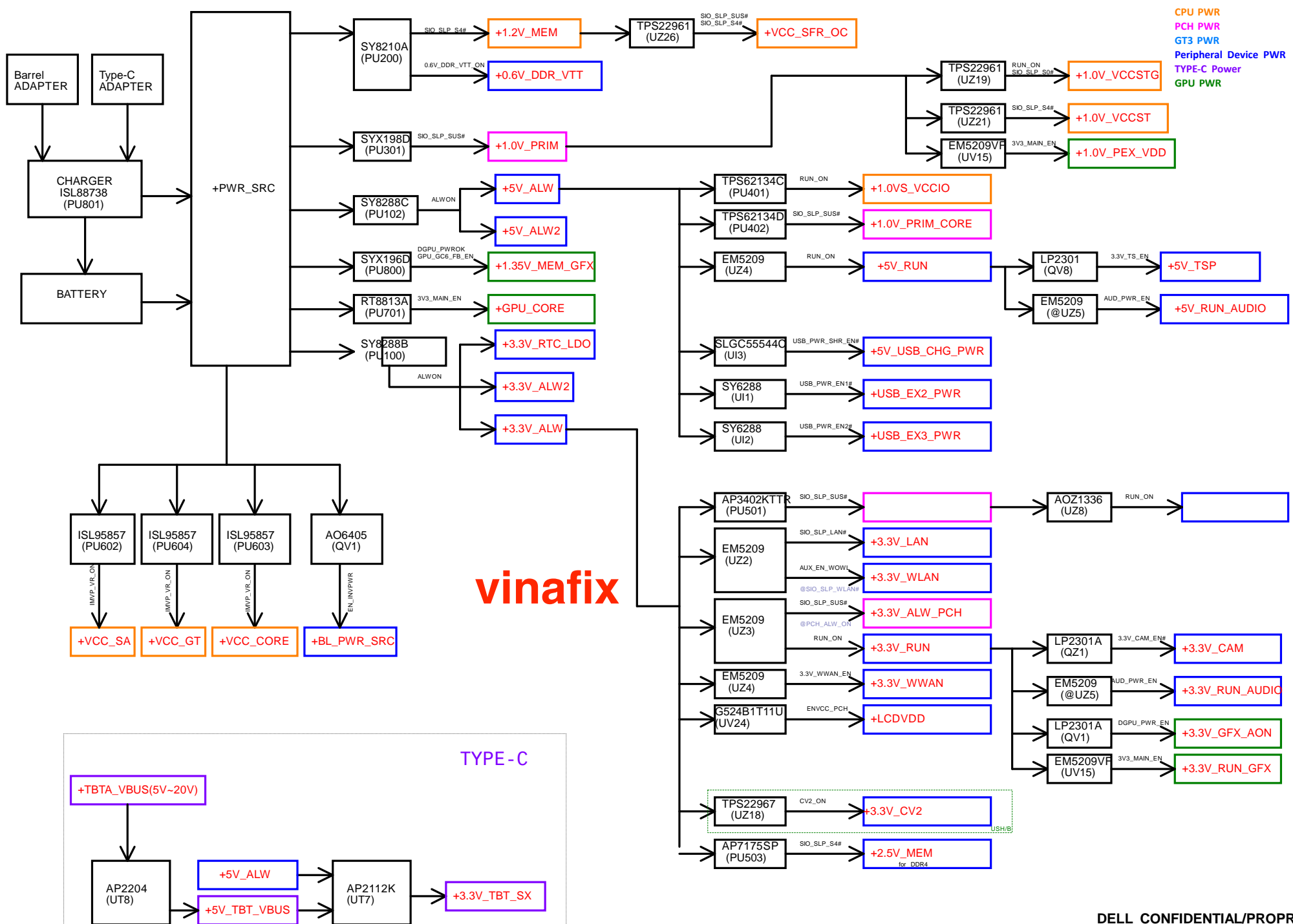
High Speed I/O (HSIO) Lane Multiplexing in KBL U



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Port assignment	
LA-E082P	
Date: Monday, December 12, 2016	Sheet 3 of 75

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CPU PWR  
PCH PWR  
GT3 PWR  
Peripheral Device PWR  
TYPE-C Power  
GPU PWR

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TYPE-C

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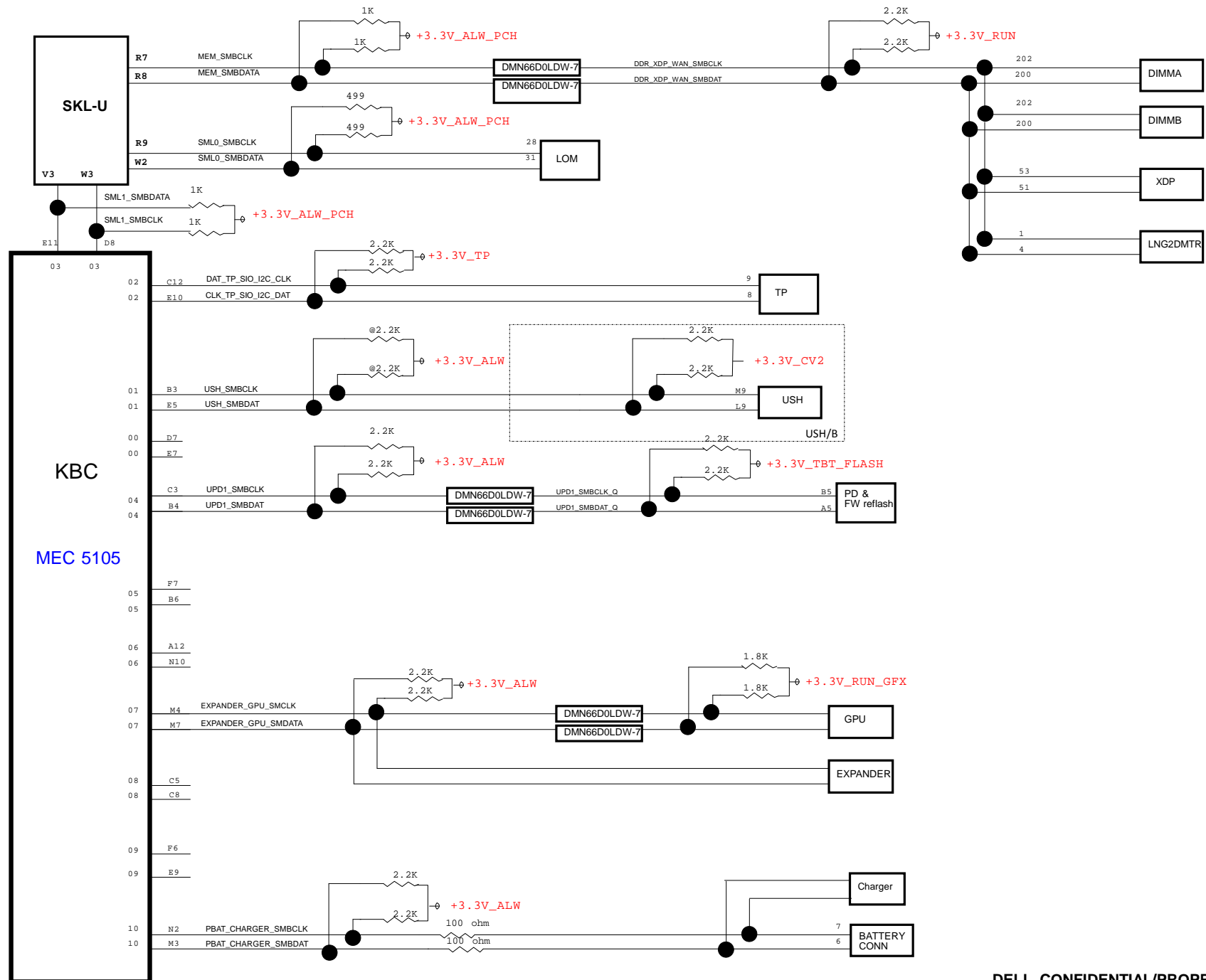
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Power rails

LA-E082P


Rev 1.0

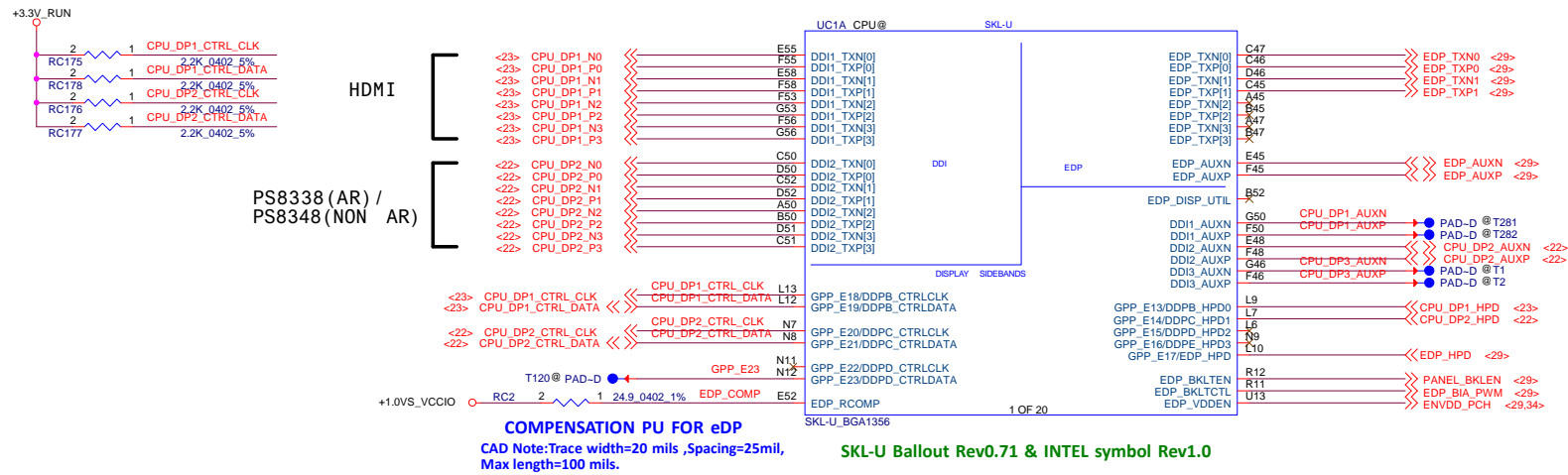
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Title	<b>Port Schematic</b>		
Size	Document	Number	Rev
			1.0
Date:	Monday, December 12, 2016	Sheet	5 of 75

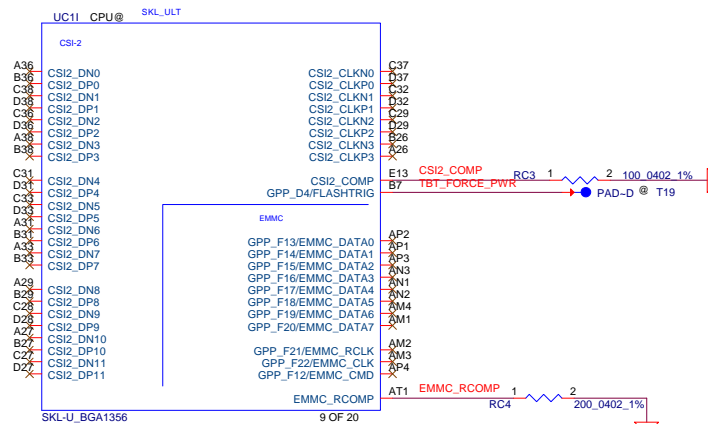


## COMPENSATION PU FOR eDP

CAD Note: Trace width=20 mils, Spacing=25mil,  
Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0

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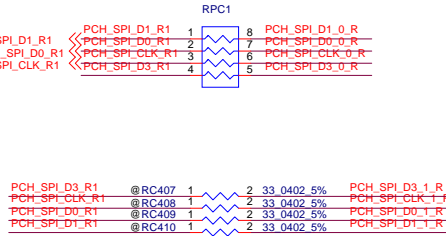
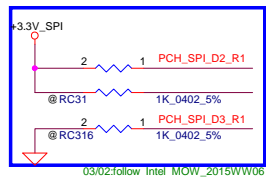
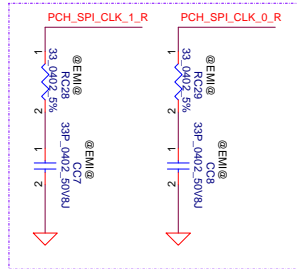
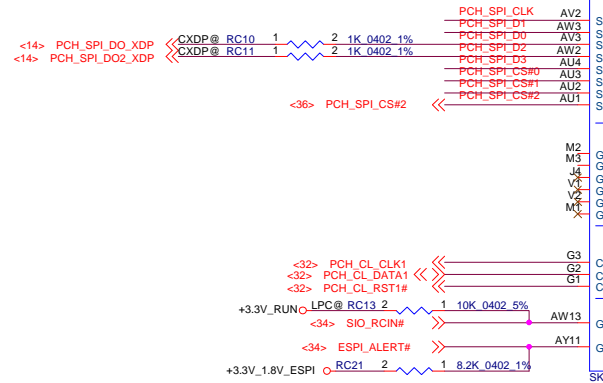


CPU (1/14)			Rev 1.0
Title	Document Number	LA-E082P	
Date: Monday, December 12, 2016	Sheet 6	of 75	

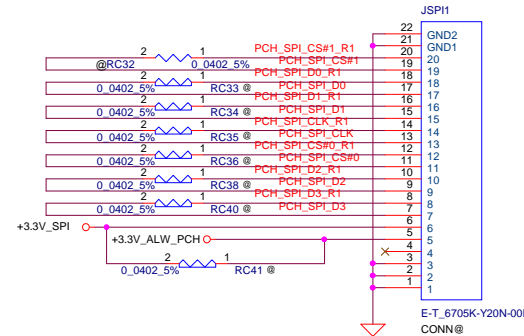
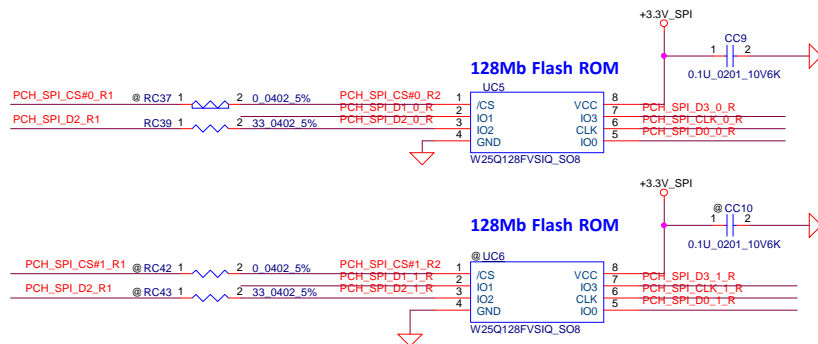
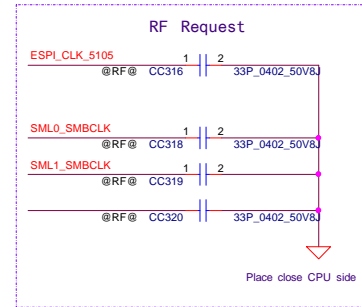
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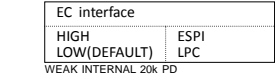
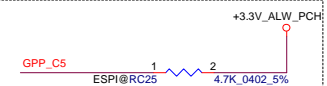
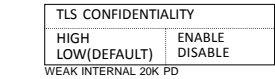
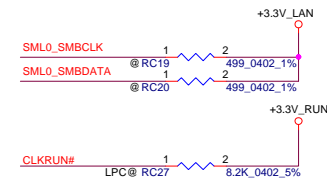
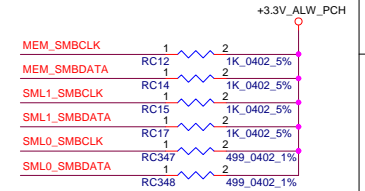
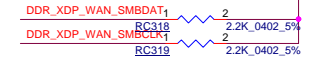
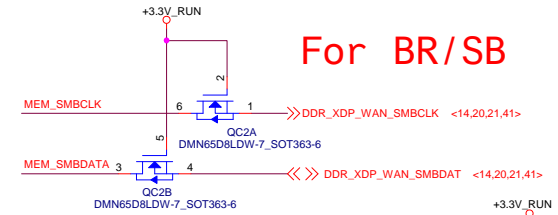
SPI\_MOSI= SPI\_IO0  
SPI\_MISO= SPI\_IO1  
PCH EDS R0.7 p.235~236



### SOFTWARE TAA



For BR/SB



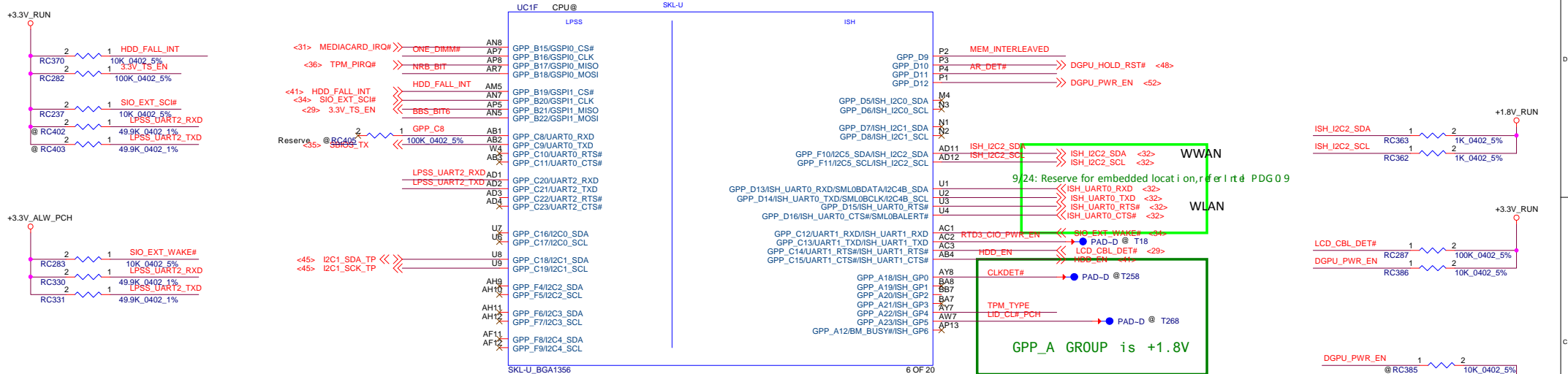
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CPU (3/14)			
LA-E082P			
Date:	Monday, December 12, 2016	Sheet	8 of 75

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For BR DSC



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CPU (4/14)

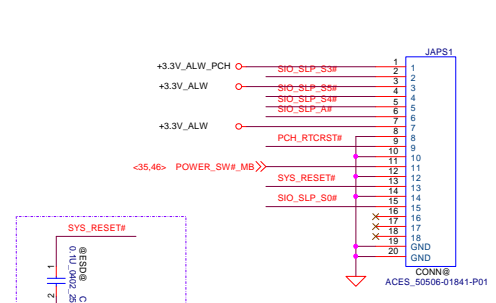
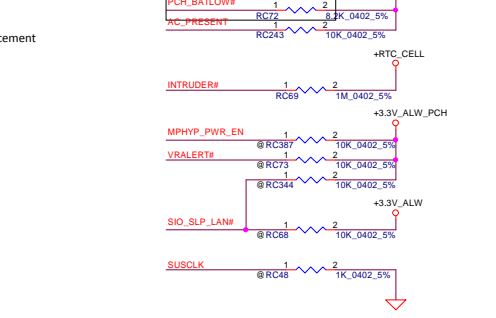
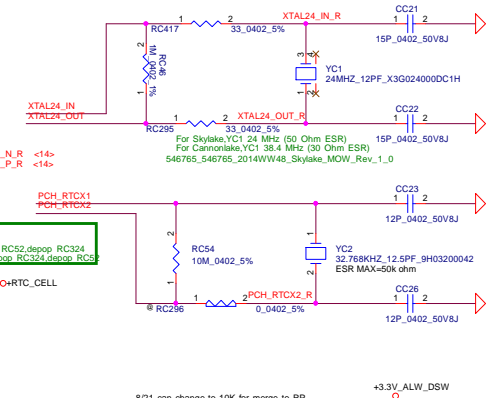
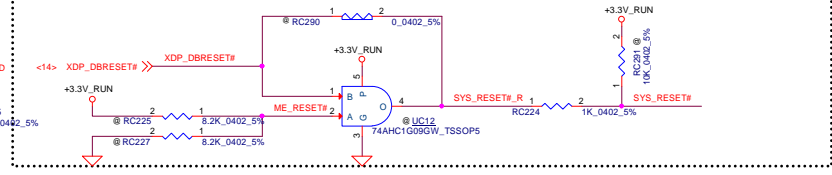
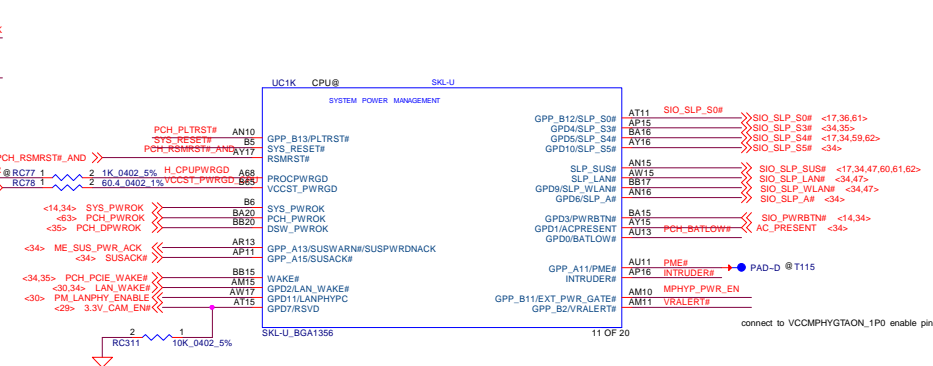
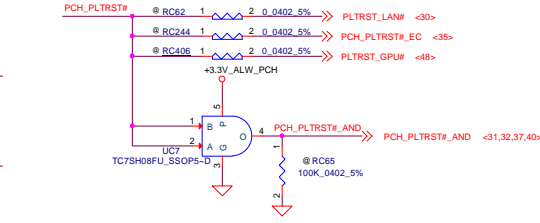
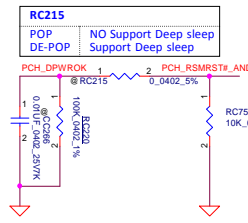
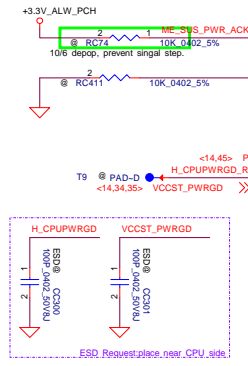
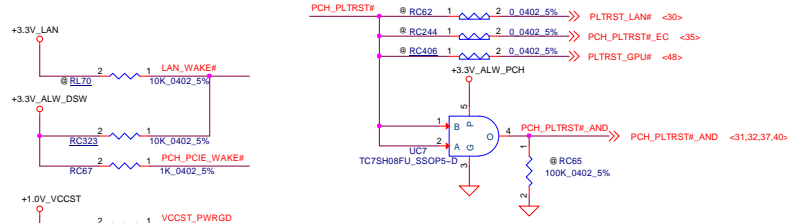
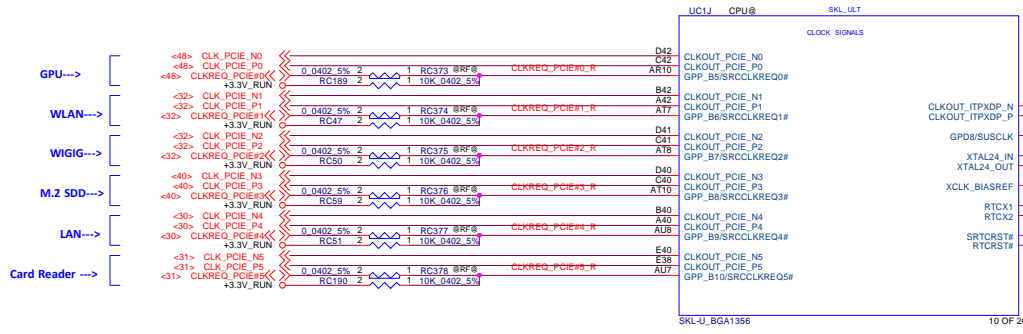
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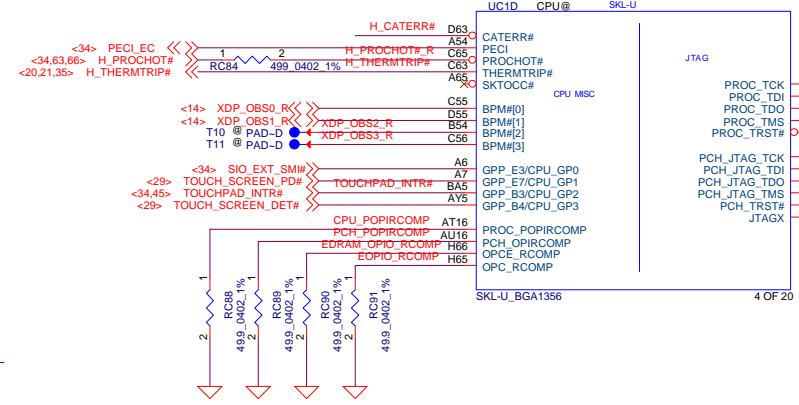
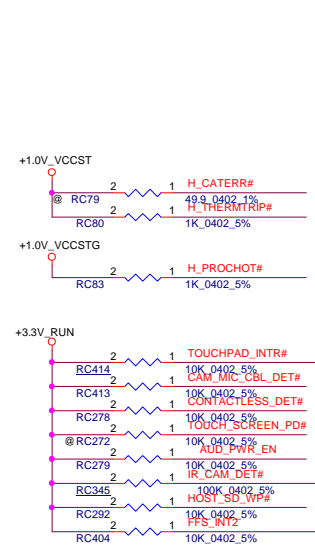
Rev 1.0

Date: Monday, December 12, 2016 Sheet 9 of 75

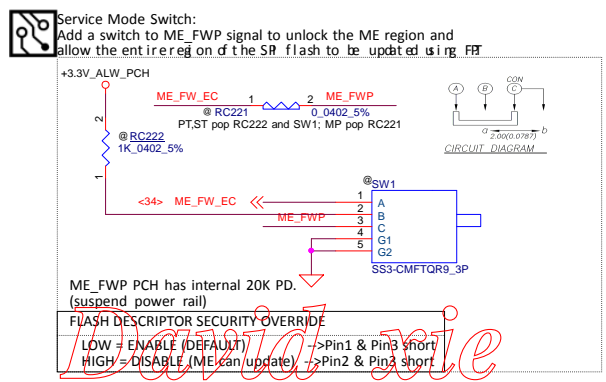
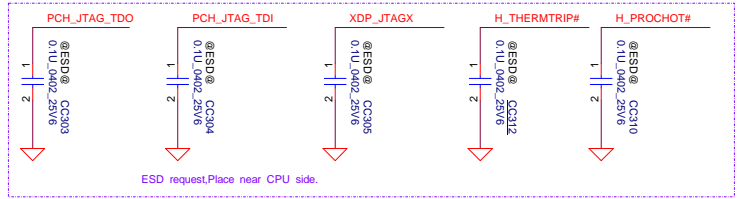
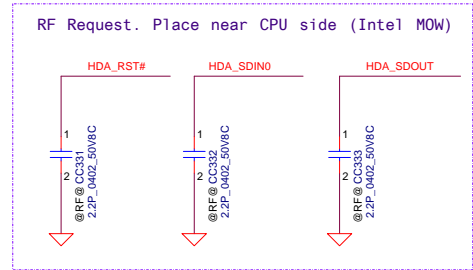
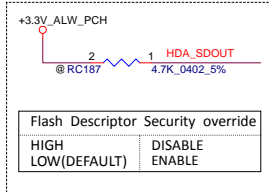
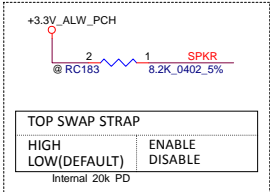
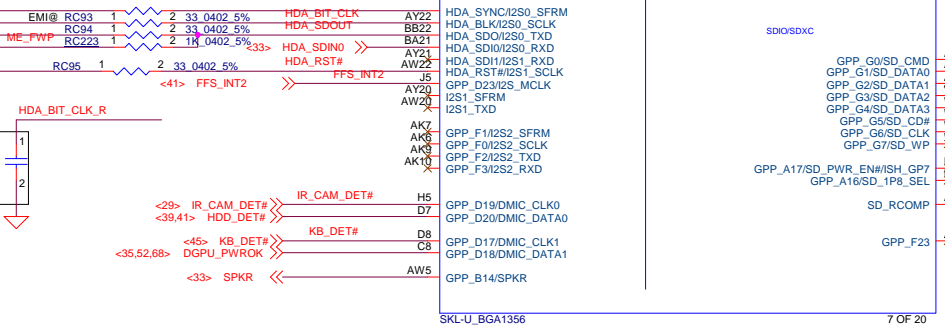


For BR DSC





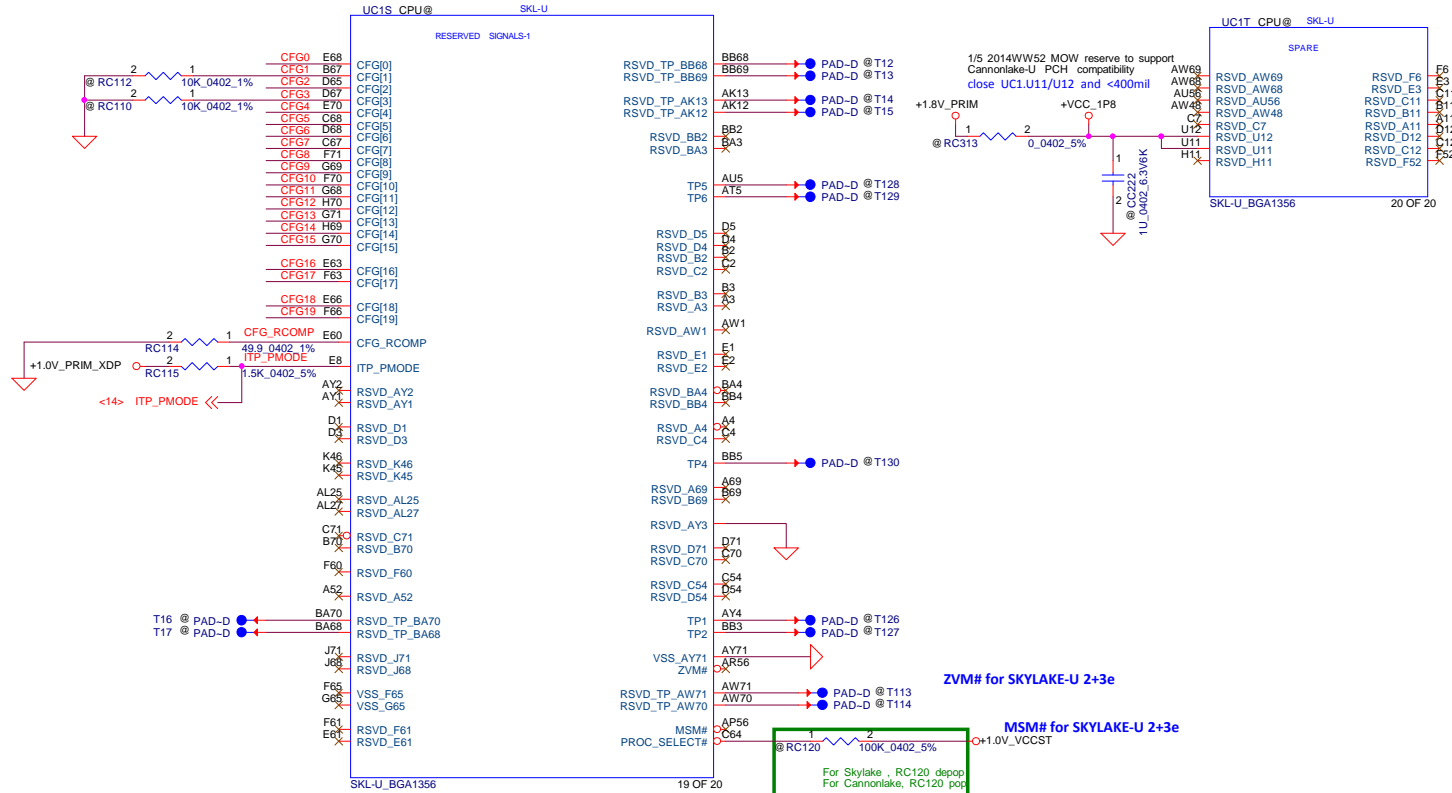
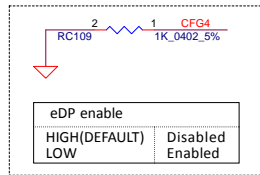
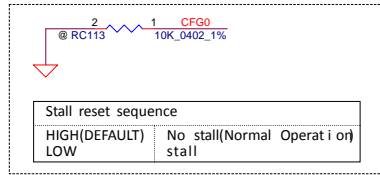
TOUCH\_SCREEN\_PD# don't move to RPC,



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<14> CFG[0..19] <<

### CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin



546765\_546765\_2014WW48\_Skylake\_MOW\_Rev\_1\_0

For Skylake , RC120 depop  
For Cannonlake, RC120 pop

PROC\_SELECT# This pin is for compatibility with future platforms. It should be unconnected for KBL

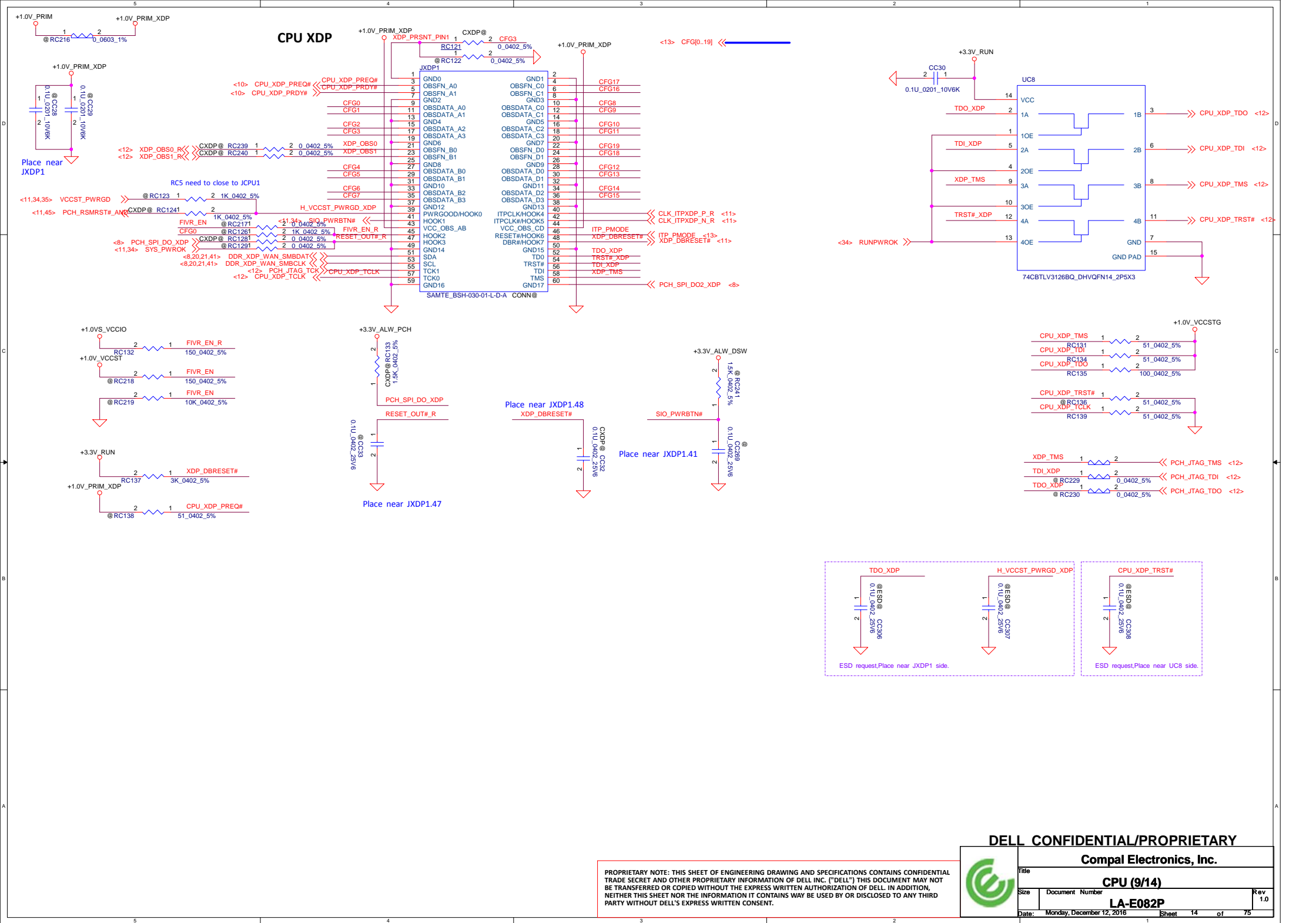
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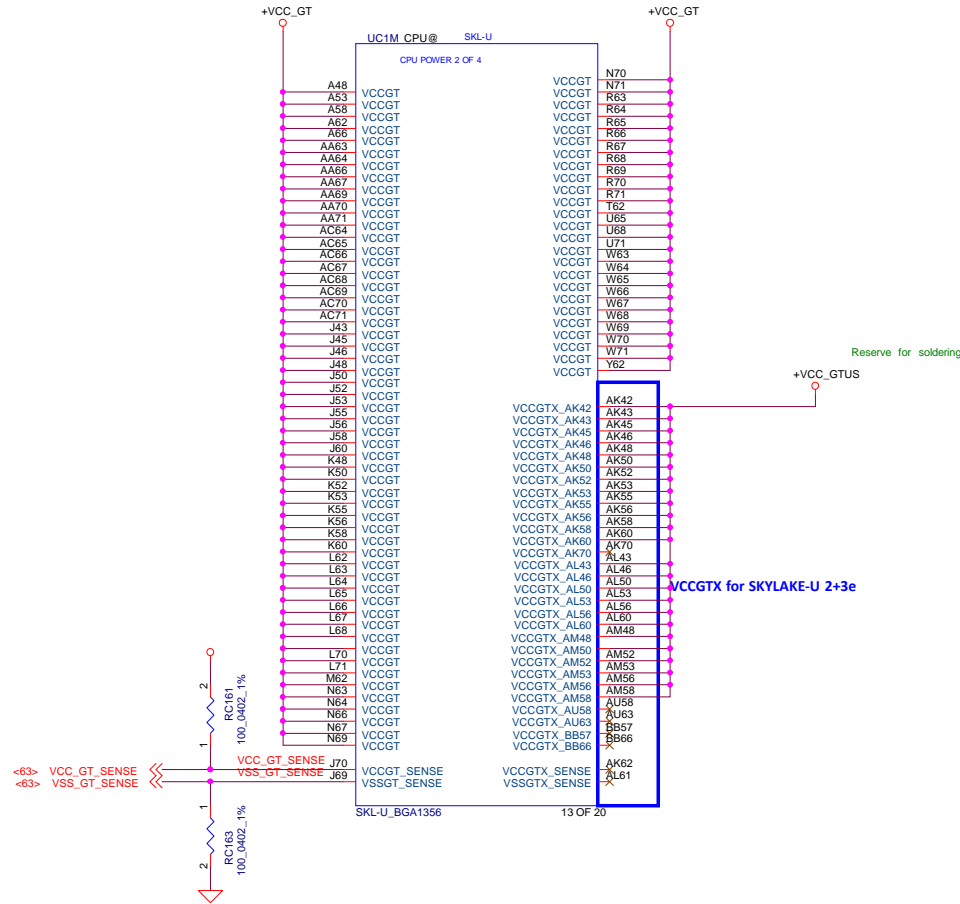
CPU (8/14)				Rev
Title	Document Number	LA-E082P		1.0
Date	Monday, December 12, 2016	Sheet	13	of 75

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+VCCGT: 0.3~1.35V  
+VCCGTX : 0.3~1.35V



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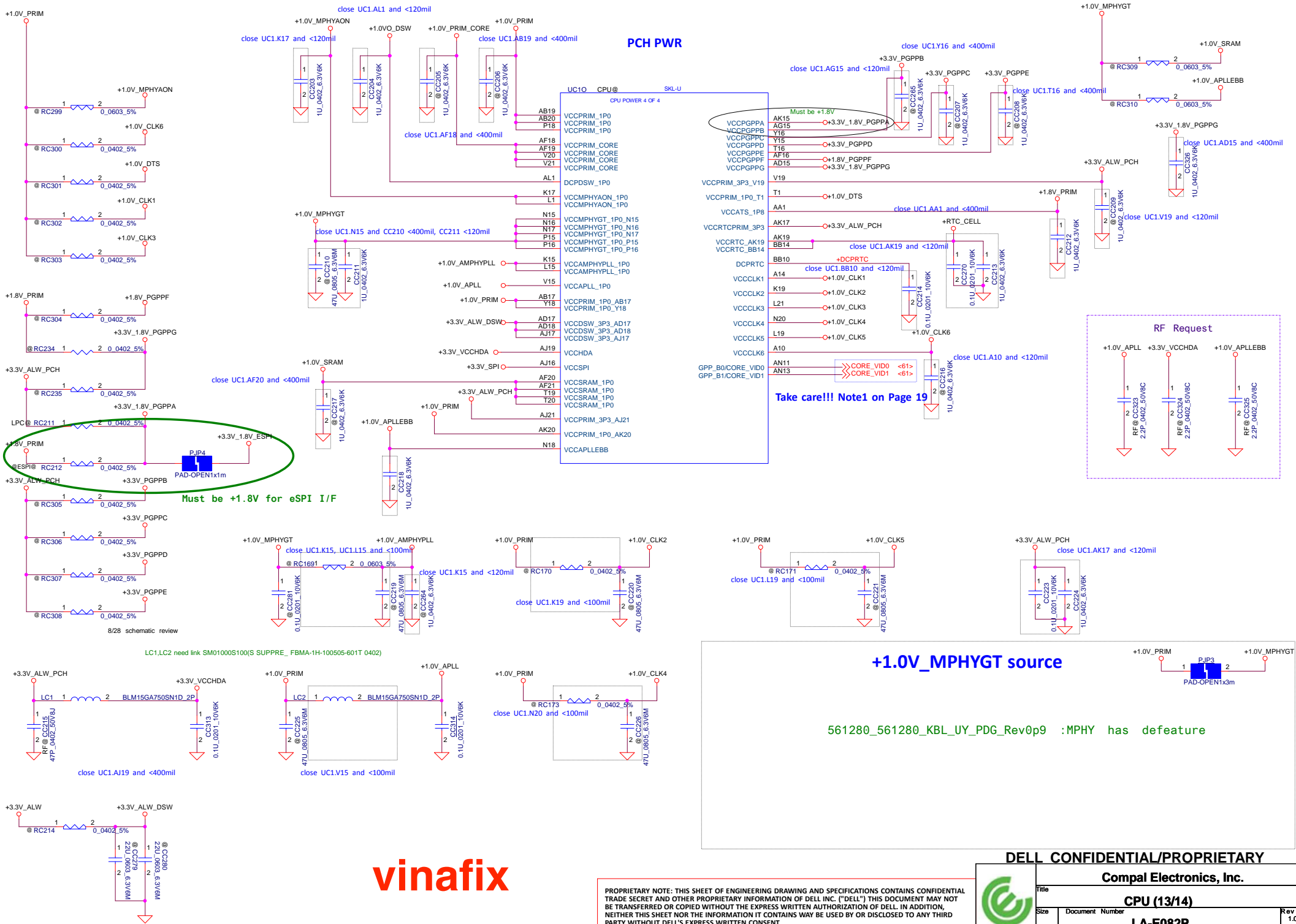
**CPU (11/14)**

**LA-E082P**

Monday, December 12, 2016

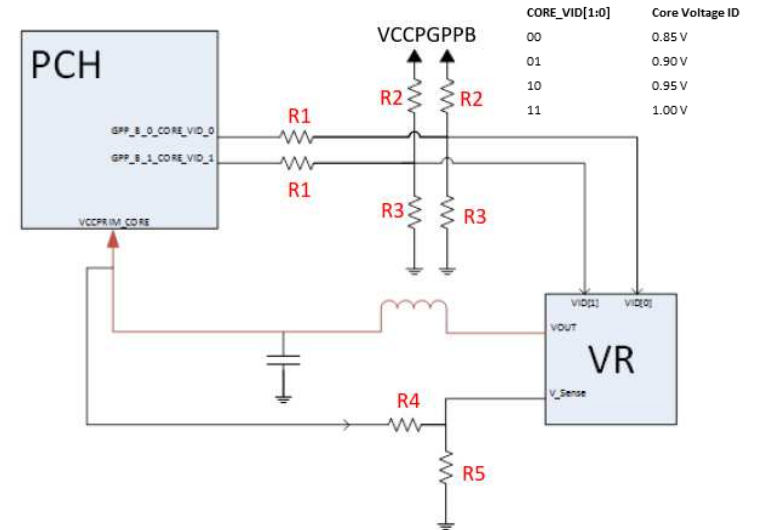
Title		Rev
Size	Document Number	1.0
Date: Monday, December 12, 2016		Sheet 16 of 75





Note1: VCCPRIM\_CORE Implementat i on w t h PCH CORE\_V D Reco mnendat i on

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



For Pre-ES Parts: Disconnect PCH CORE\_VID[1:0] to the VR and fix PCH VCCPRIM\_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM\_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE\_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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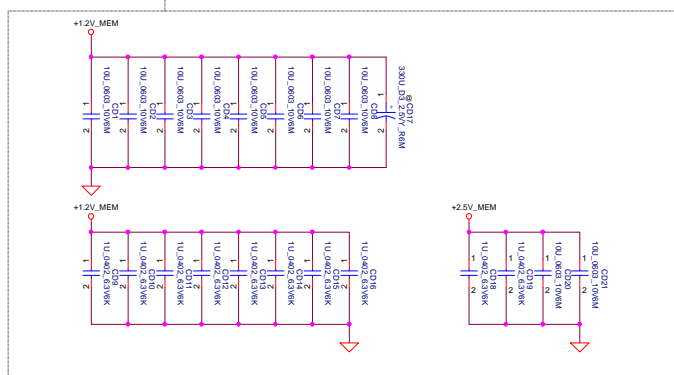


Title			
CPU (14/14)			
Size	Document Number	Rev	
	LA-E082P	1.0	
Date:	Monday, December 12, 2016	Sheet	19 of 75

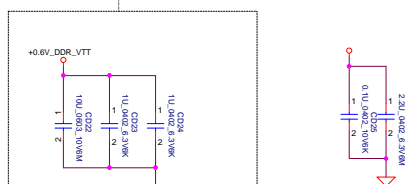
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```
<7> DDR_A_DQS#[0..7] << >>
<7> DDR_A_D[0..63] << >>
<7> DDR_A_DQS[0..7] << >>
<7> DDR_A_MA[0..16] >>
```

Layout Note:  
Place near JDIMM1

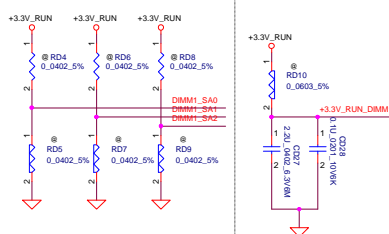


Layout Note:  
Place near  
JDIMM1.258

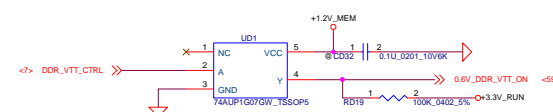
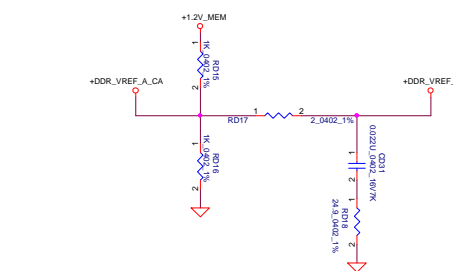
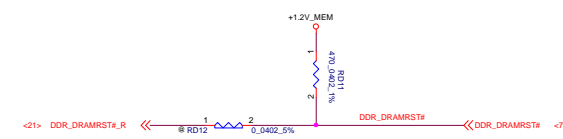
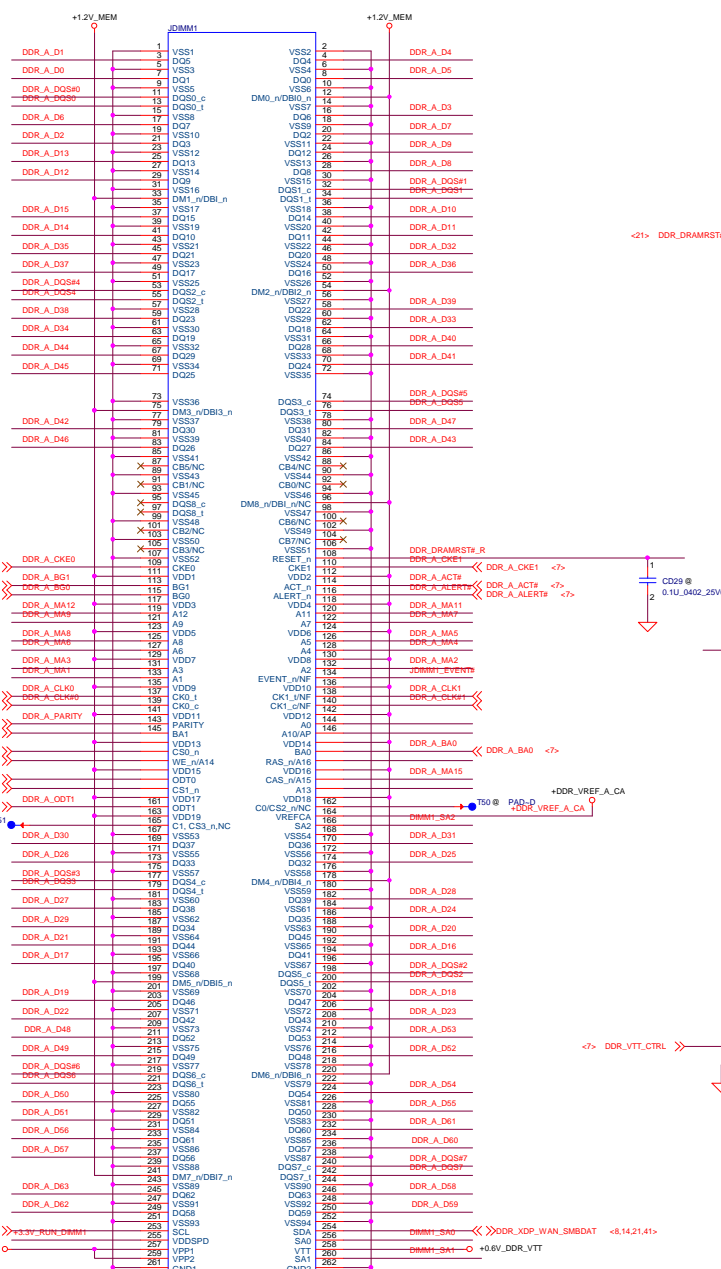


## DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



LCN\_DAN05-Q0406-0103  
CONN@  
**LINK DAN05-Q0406-0103 DONE**



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## DDR4

Size	Document Number
	LA-E0825

LA-E082P

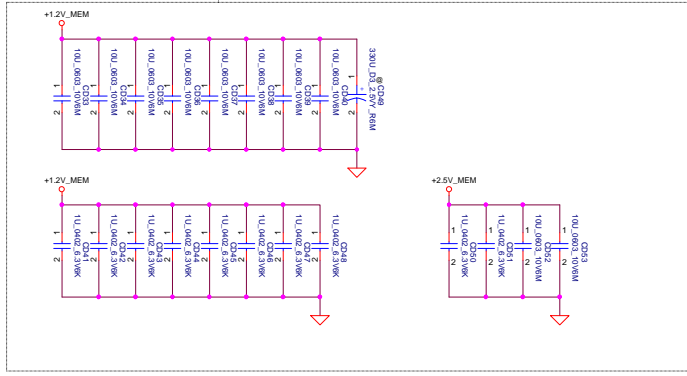
Date: Monday, December 12, 2018 Sheet 20 of 75

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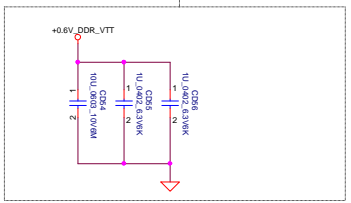


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<7> DDR\_B\_DQ[0..63] <<>  
<7> DDR\_B\_DQS[0..7] <<>  
<7> DDR\_B\_MA[0..16] <<>

Layout Note:  
Place near JDIMM2

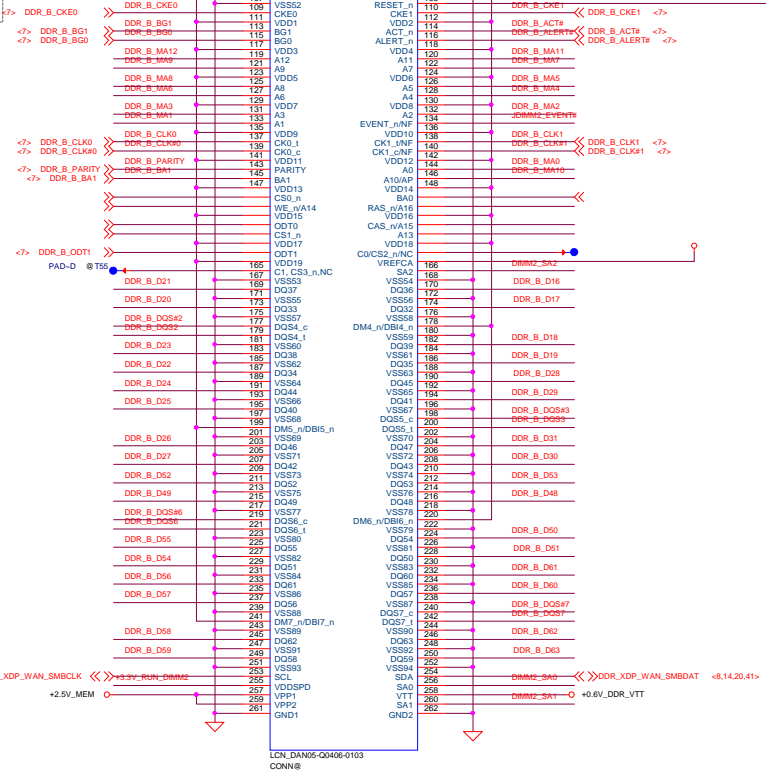
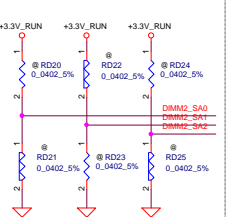


Layout Note:  
Place near JDIMM2.258



DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
* DIMM3	0	1	0
DIMM4	1	1	0



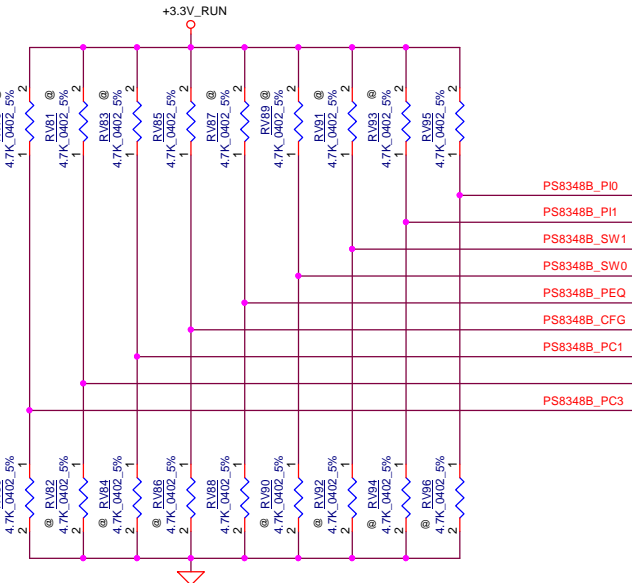
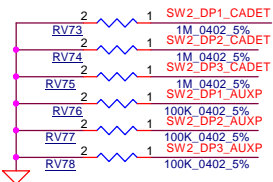
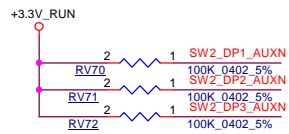
LINK DAN05-Q0406-0103 DONE

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DDR4			
Rev	1.0	LA-E082P	
Date	Monday, December 12, 2016	Sheet	21 of 76

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Internally tied to VDD33/2 3.3V I/O

PCx = M: Port output configuration is set by link training (default)

H: Port output with fixed 800 mV and 0dB

L: Port output with fixed 400 mV and 0dB

x=1, 2, 3

Internally pull down ~150K 3.3V I/O

For Control Switching Mode (CFG = L):

[SW1,SW0] = [L,L], Port1 is selected (default)

[SW1,SW0] = [L,H], Port2 is selected

[SW1,SW0] = [H,L], Port3 is selected

[SW1,SW0] = [H,H], Port3 is selected

For Automatic Switching Mode (CFG = H):

[SW1,SW0] = [L,L], Port1 > Port2 > Port3 (default)

[SW1,SW0] = [L,H], Port1 > Port3 > Port2

[SW1,SW0] = [H,L], Port3 > Port2 > Port1

[SW1,SW0] = [H,H], Port3 > Port1 > Port2

[SW1,SW0] = [L,M], Port2 > Port1 > Port3

[SW1,SW0] = [M,M], Port2 > Port3 > Port1

PI0: Automatic EQ disable Internal pull down ~150K ohm 3.3V I/O

PI0 = L: Automatic EQ enable (default)

H: Automatic EQ disable

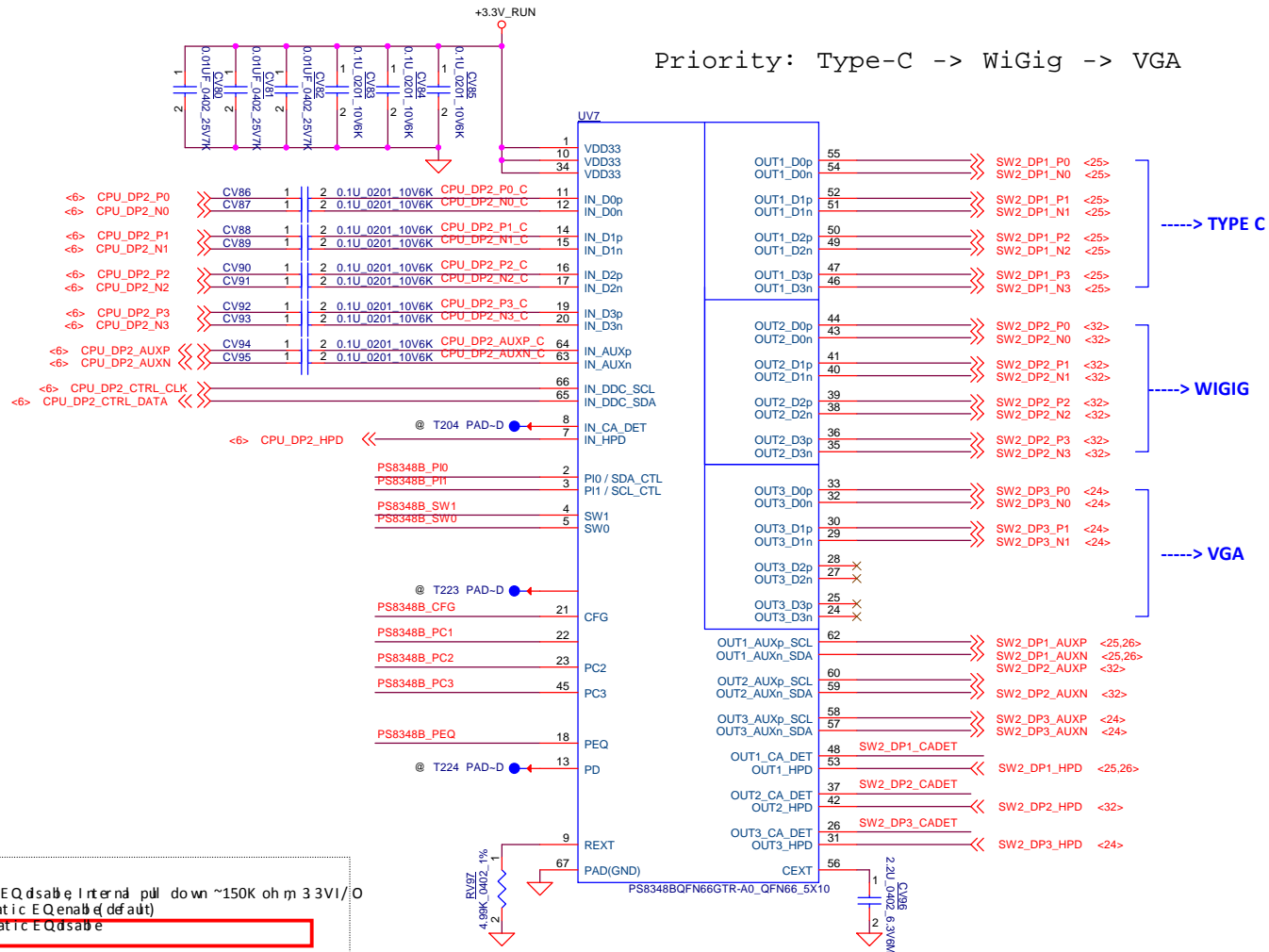
Internally tied to VDD33/2 3.3V I/O

PEQ =

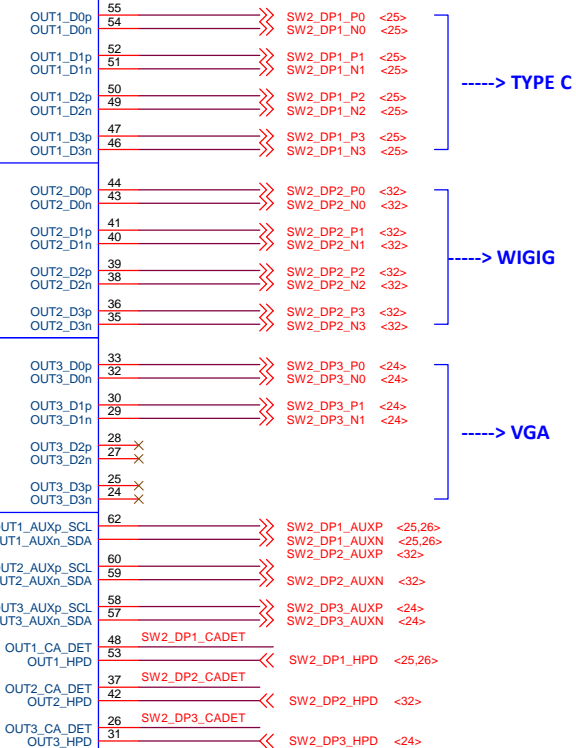
M: default, LEQ, compensate channel loss up to 11.5dB @ HBR2

H: HEQ, compensate channel loss up to 14.5dB @ HBR2

L: LLEQ, compensate channel loss up to 8.5dB @ HBR2



Priority: Type-C -> WiGig -> VGA

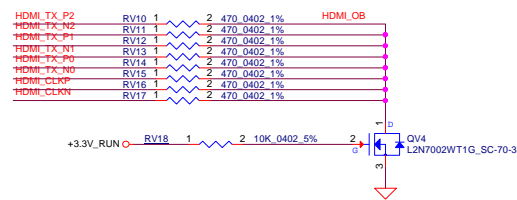
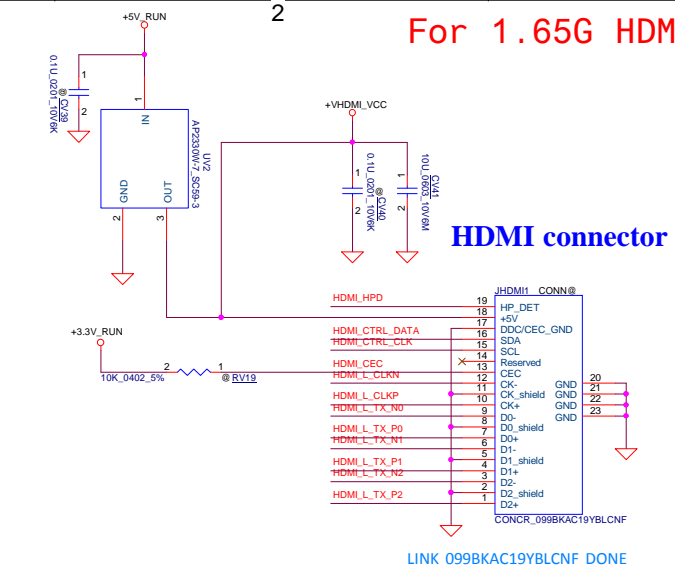
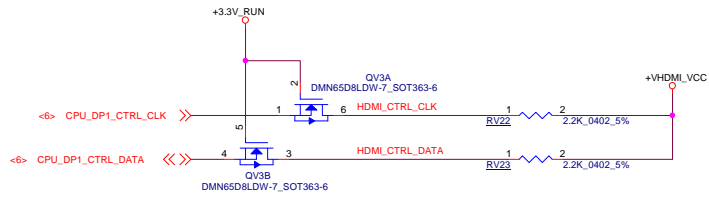
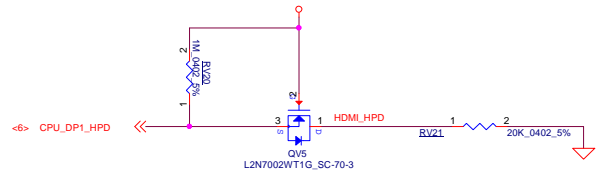
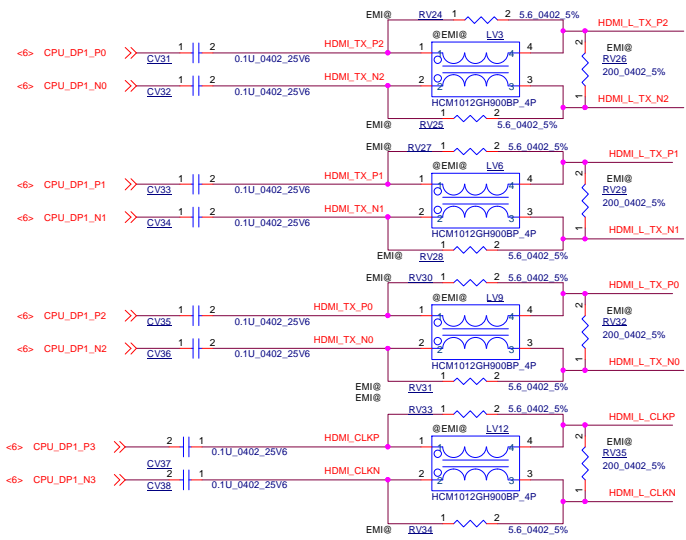


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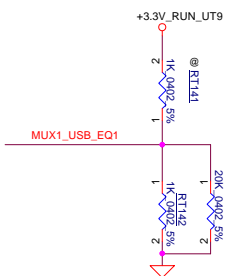
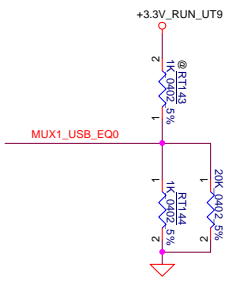
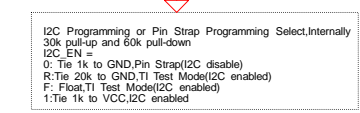
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Size	Document Number	Rev	
		1.0	
Date:	Monday, December 12, 2016	Sheet	22 of 75

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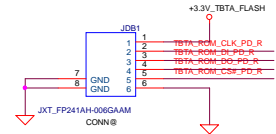
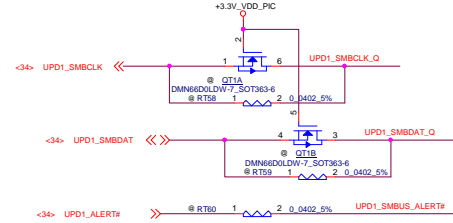
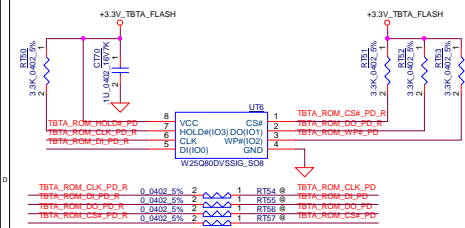




USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

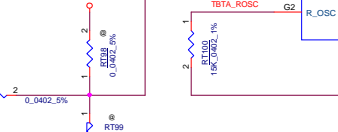
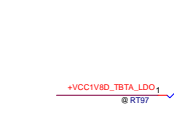
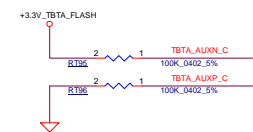


Date: Monday, December 12, 2016 Sheet 25 of 75



DIV = R2/(R1+R2)	Factory Configuration	Device Configuration	Description
0.00	0.08	0	UFP only 5V @3.0A Sink capability with 'Ask for Max' for anything from 0.9 - 3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @3.0A Sink capability with 'Ask for Max' for anything from 0.9 - 3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Sink capability with 'Ask for Max' for anything from 0.9 - 3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Sink capability with 'Ask for Max' for anything from 0.9 - 3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps but will not initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps but will not initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host IF cycles.

Route in pass through manner so AUX can be snooped by 546



Link TPS65982D (from SA00009W200 to SA00009W210) 08/04

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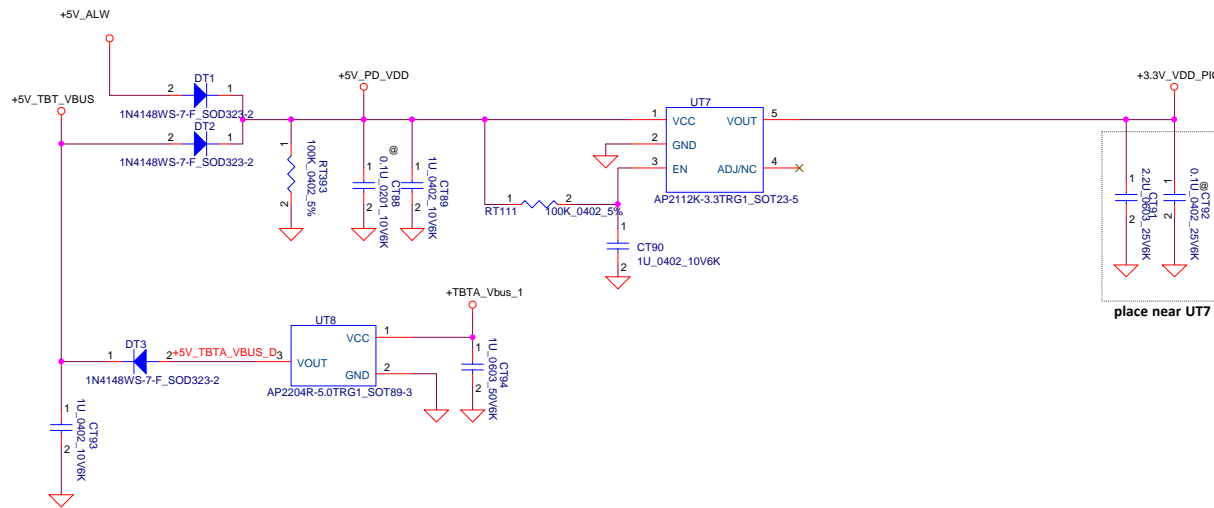
Type CIPD Controller TI

LA-E082P

Date: Monday, December 12, 2016 Sheet 26 of 76

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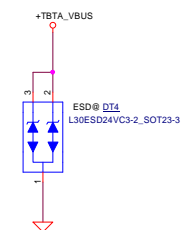
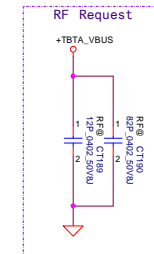
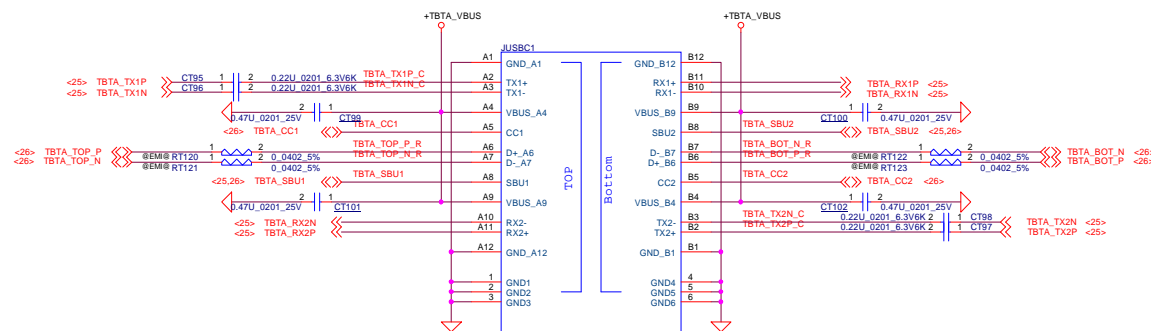




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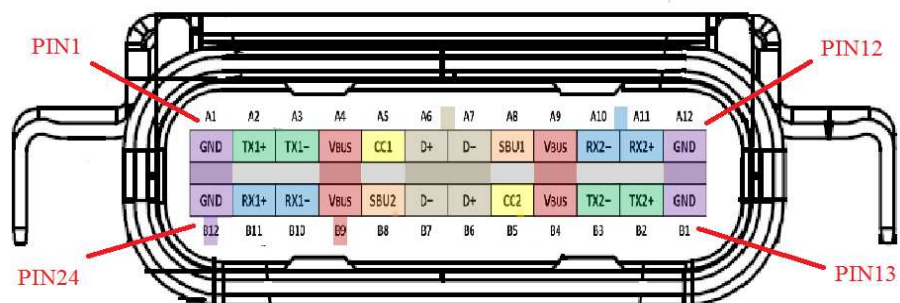
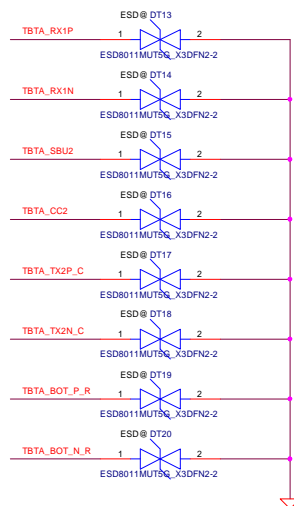
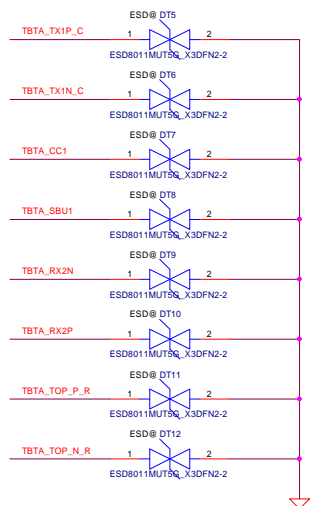


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Compal Electronics, Inc.			
Title		[Type C]PD Power	
Size	Document Number	Rev	
		LA-E082P	
Date:	Monday, December 12, 2016	Sheet	27 of 75



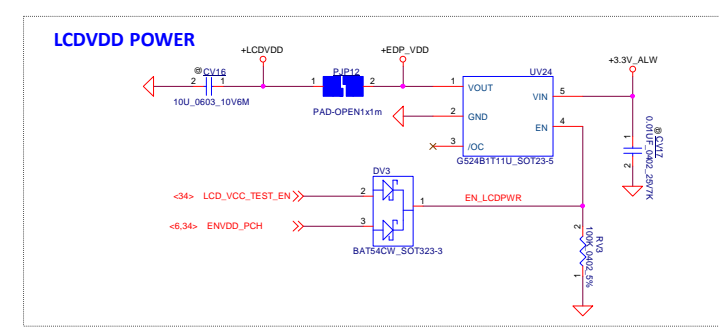
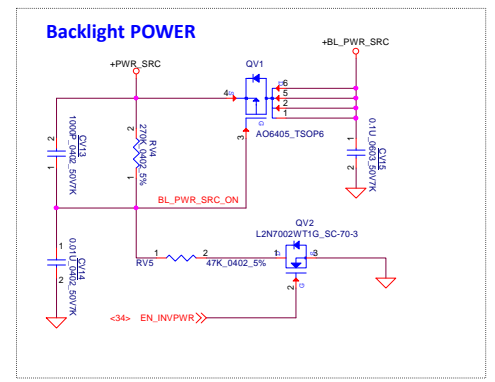
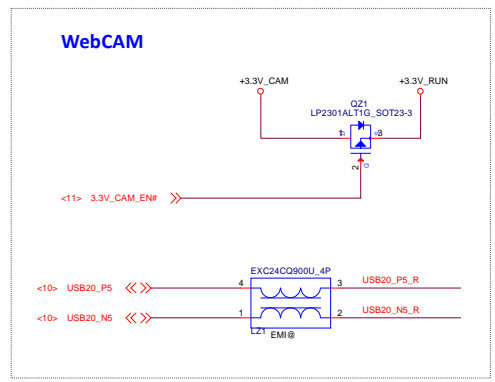
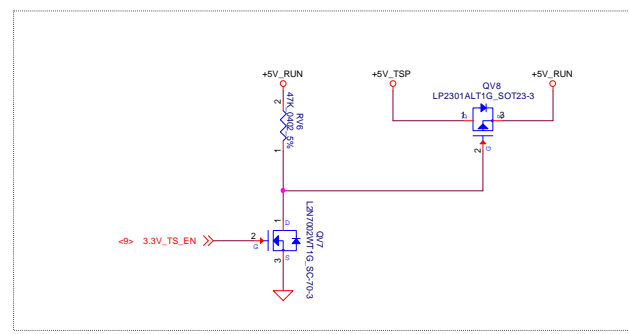
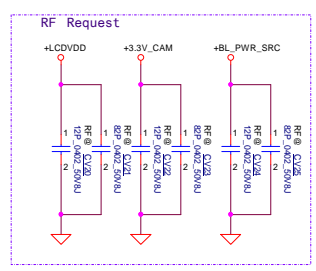
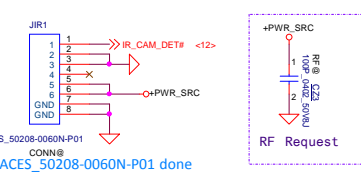
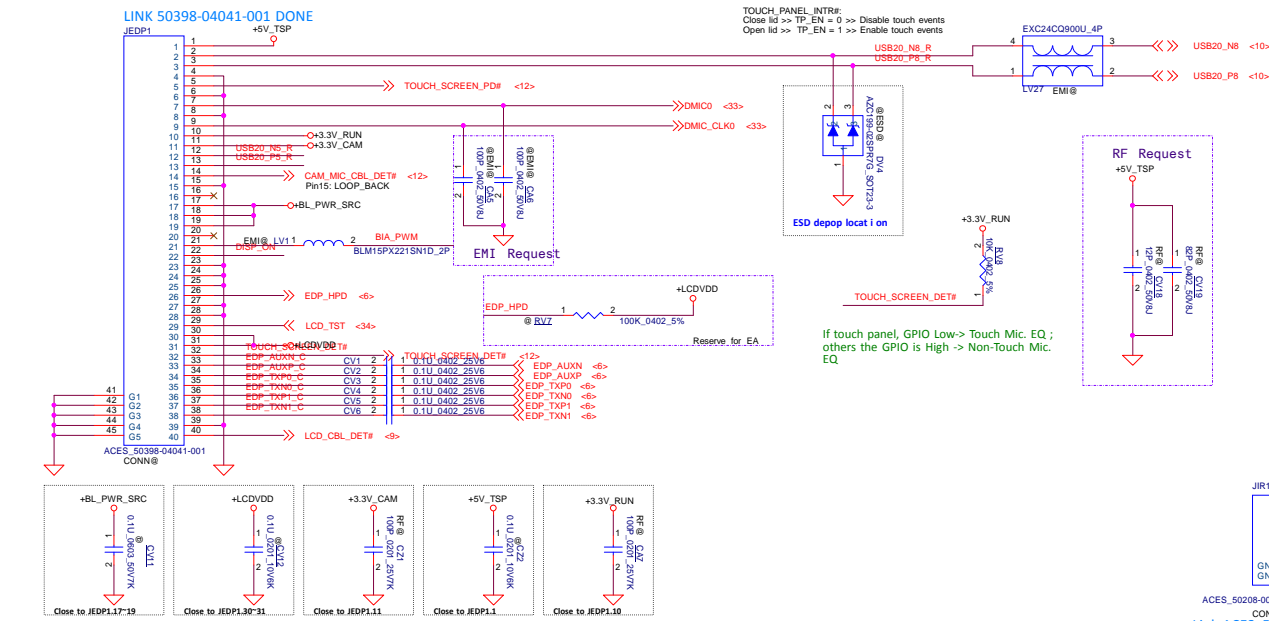
### DX07BD24JJ2 LINK DONE

Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B



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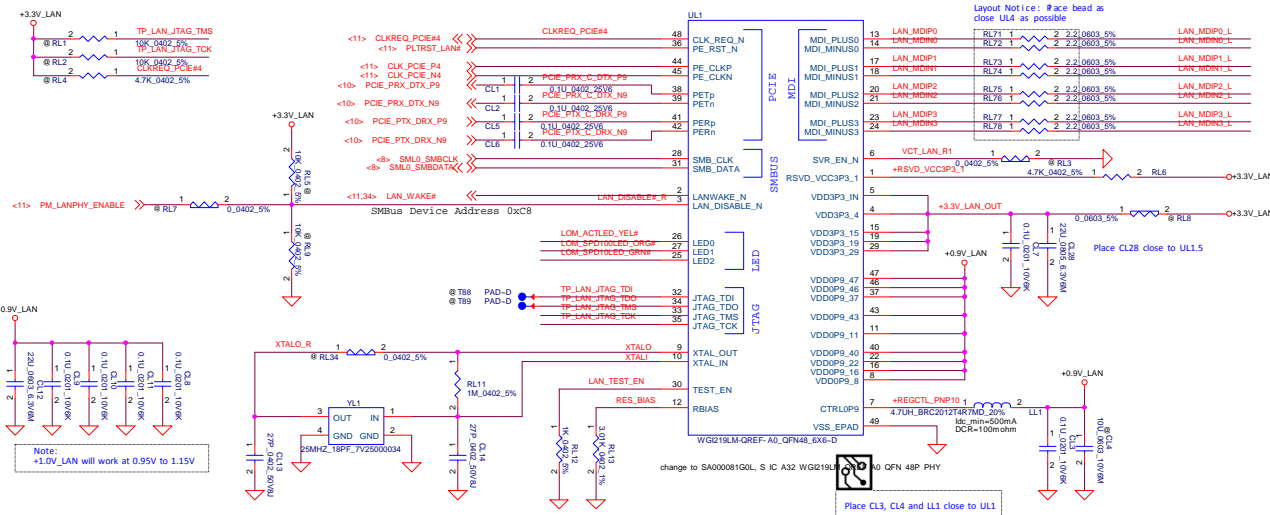
For 2LANE EDP & 5V\_TSP  
For Breckenridge 14/15



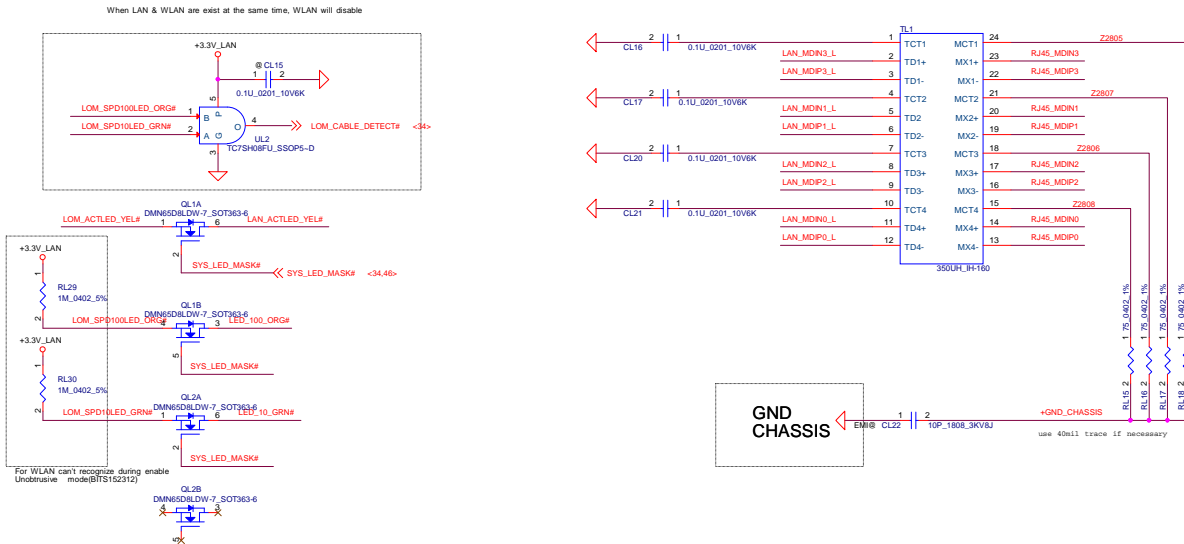
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Compal Electronics, Inc.		
eDP CONN & Touch screen		
File	Document Number	Rev
Size	LA-E082P	1.0
Date	Monday, December 12, 2016	Sheet 29 of 75

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vinafix



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Compal Electronics, Inc.

LAN Clarkville & RJ45

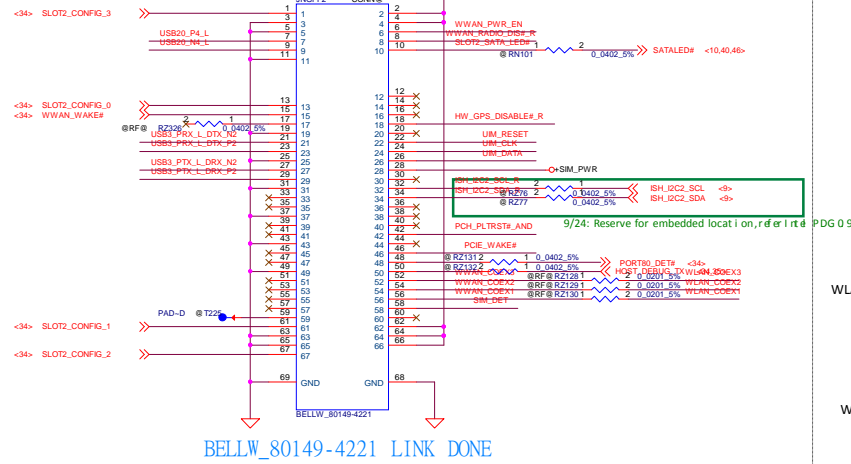
LA-E082P

Date: Monday, December 12, 2016 Sheet 30 of 75

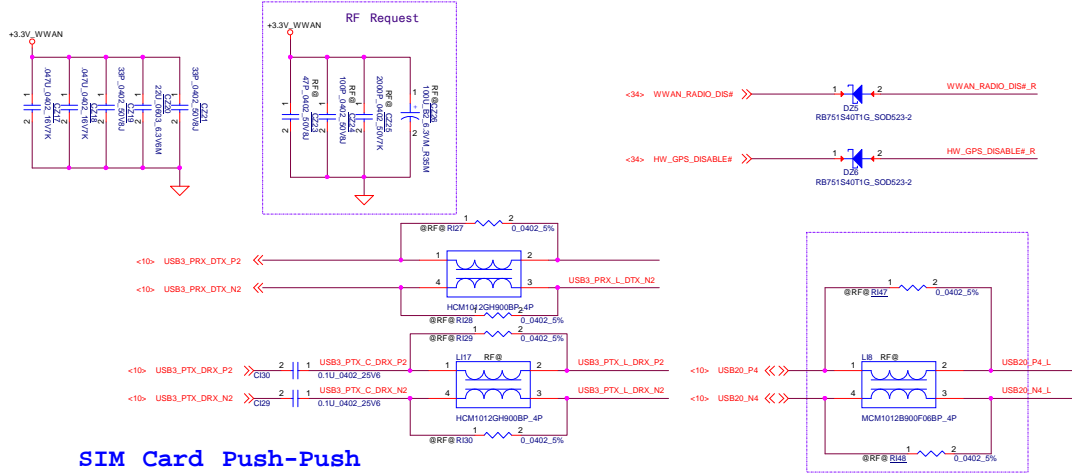
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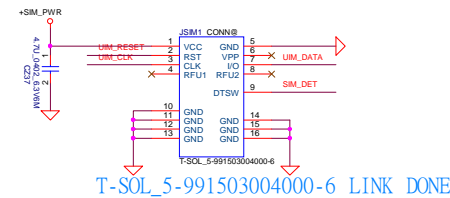
## NGFF slot B Key B



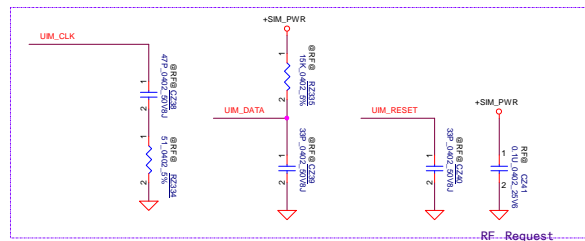
BELLW\_80149-4221 LINK DONE



## SIM Card Push-Push

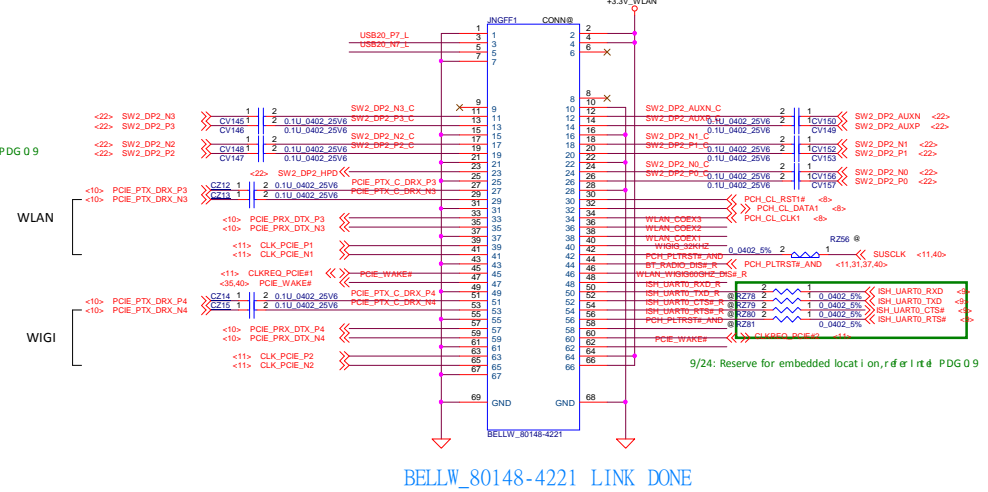


T-SOL\_5-991503004000-6 LINK DONE

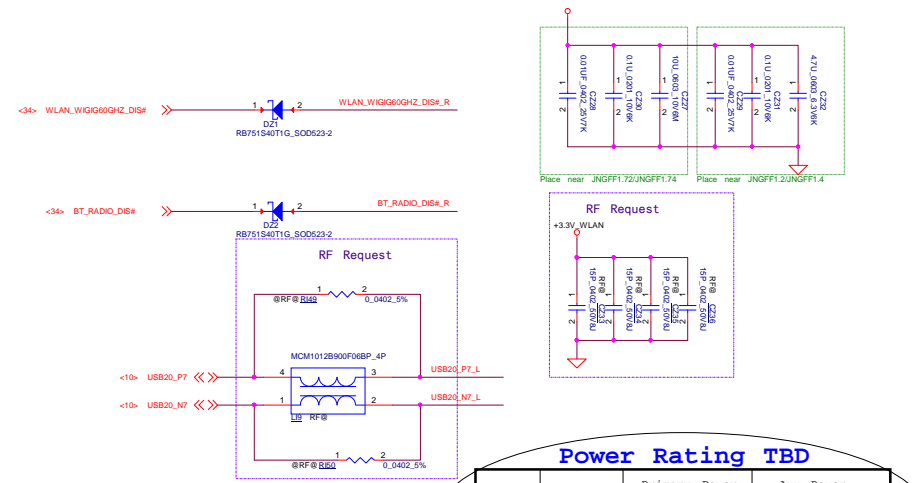


for Breckenridge 14/15 DSC

## NGFF slot A Key A



BELLW\_80148-4221 LINK DONE



## Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power	Aux Power
+3.3V		Peak	Normal

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NGFF Card

LA-E082P

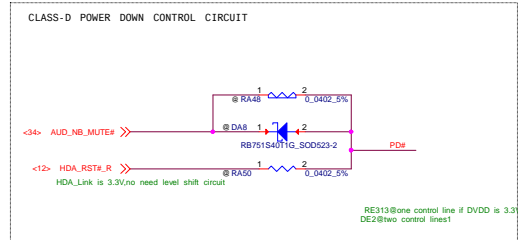
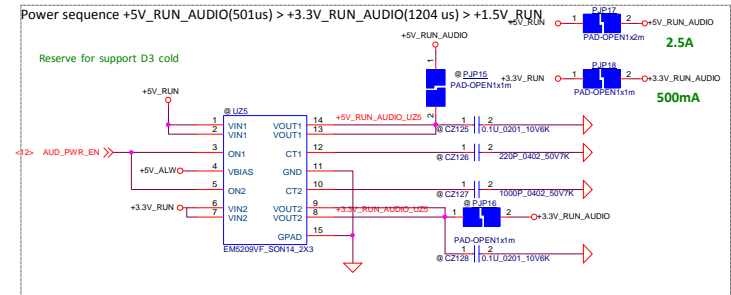
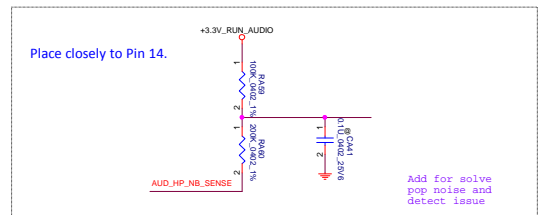
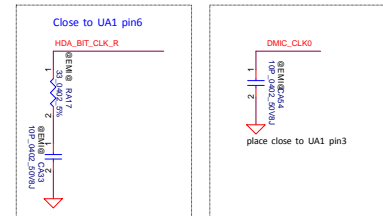
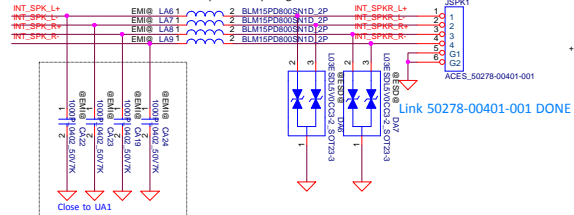
Monday, December 12, 2016 Sheet 32 of 75

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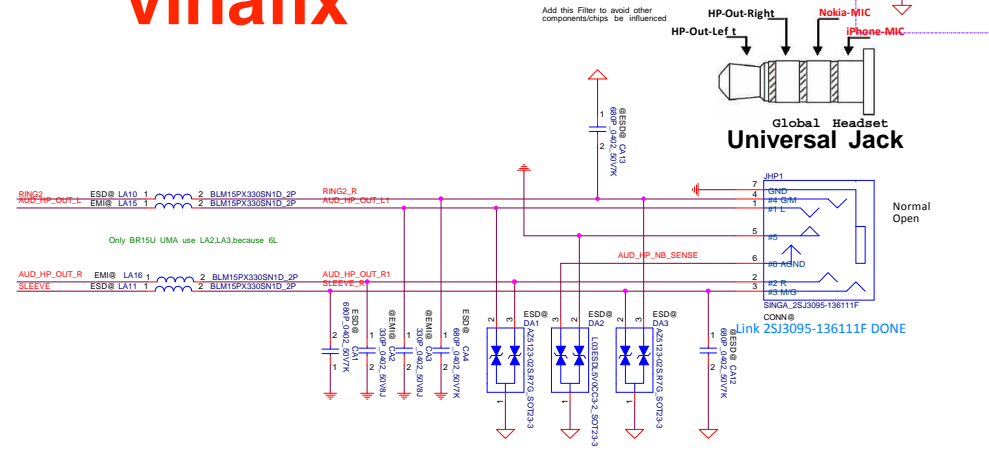
1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box)

## Internal Speakers Header

40 mils trace keep 20 mil spacing

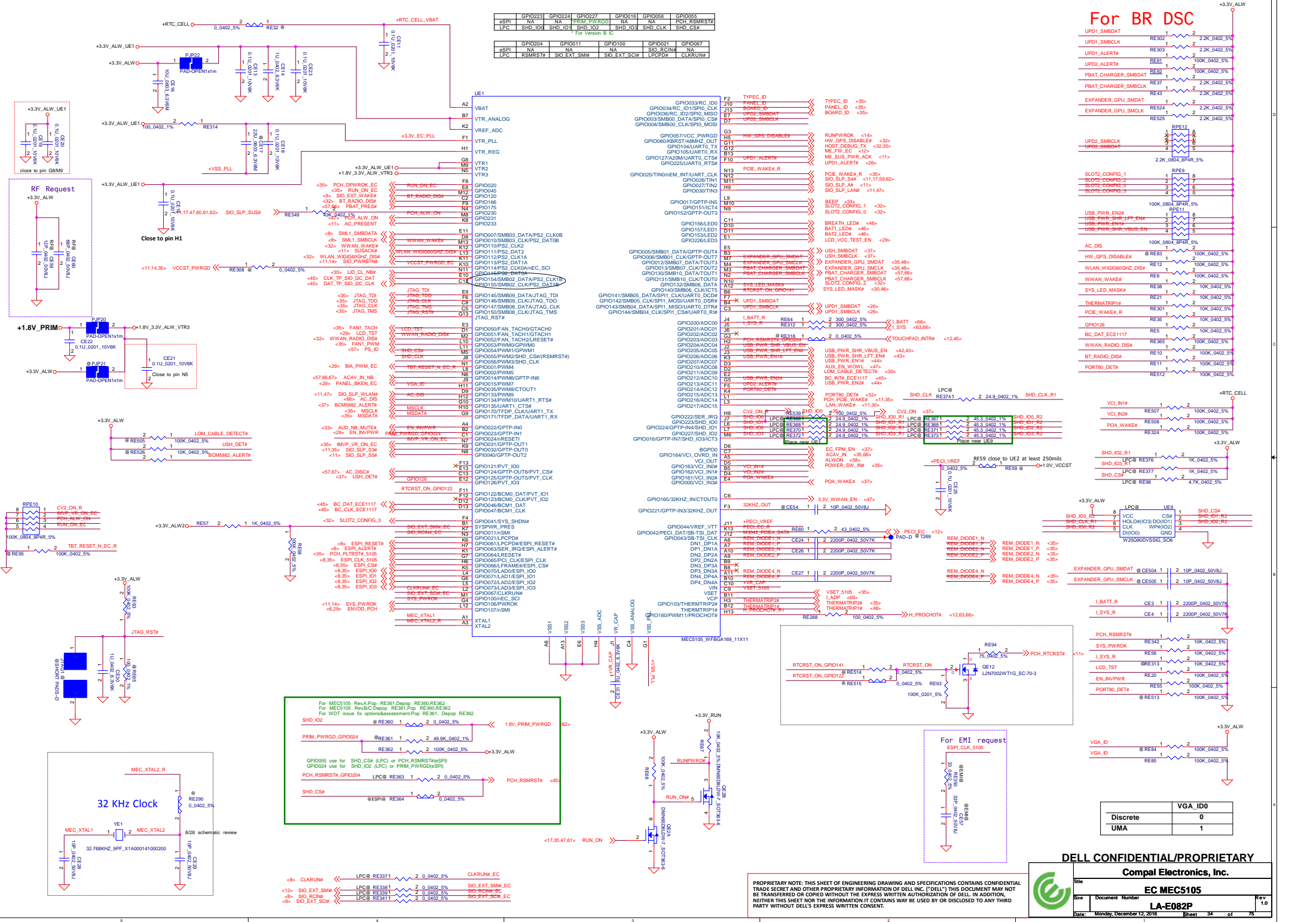


# vinafix

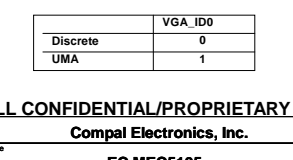
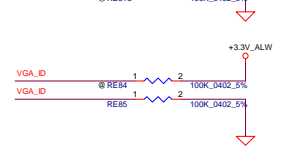
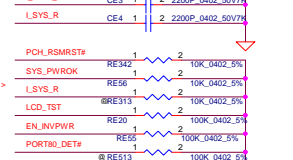
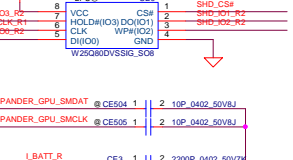
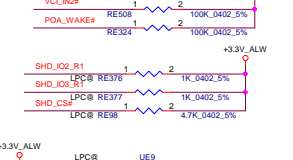
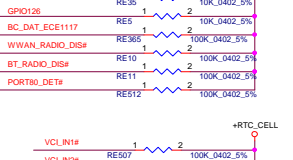
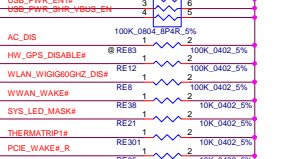
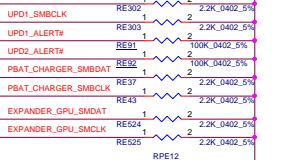


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Compal Secret Data			
Issued Date	2016/01/01	Deciphered Date	<Deciphered_Date>
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Rev	1.0	Document Number	LA-E082P
Date	Monday, December 12, 2016	Sheet	33 of 75

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Codec ALC3246



For BR DSC

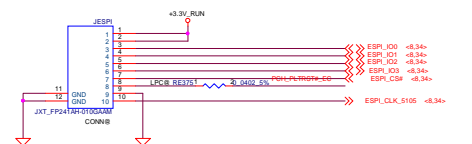
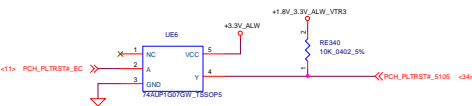


Discrete		UMA
0		1

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EC MEC5105  
LA-E082P  
Date: Monday, December 12, 2016 Sheet 34 of 78

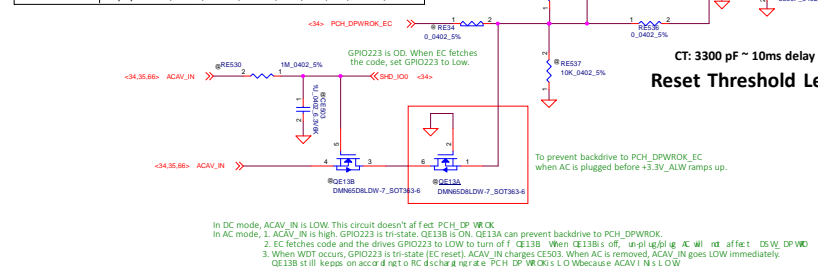
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JXT\_FP241AH-010GAAM LINK DONE

LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_I00
4	LPC_LAD1	ESPI_I01
5	LPC_LAD2	ESPI_I02
6	LPC_LAD3	ESPI_I03
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

WDT opt1 on
MECS105 rev.B
Pop RE361, QE13, CE503, RE530, UE7, CE5, CE6, RE348
Depop RE362, RE536, RE537
MECS105 rev.C
Pop RE362, RE536,
Depop RE361, QE13, CE503, RE530, UE7, CE5, CE6, RE348, RE537



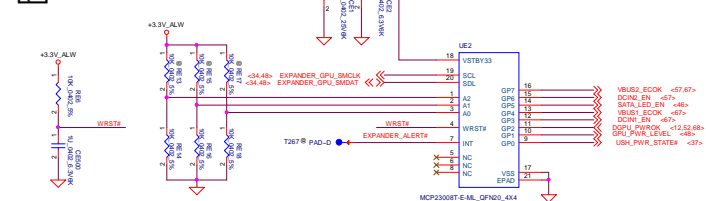
## Control Byte

R/W	0	1	0	0	A2	A1	A0	R/W
-----	---	---	---	---	----	----	----	-----

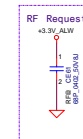
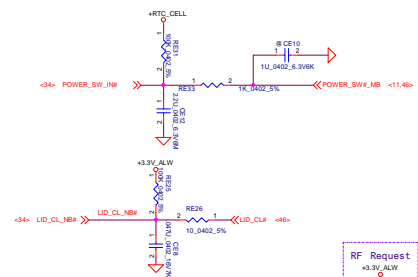
R/W = 0 = Write

R/W = 1 = Read

SMBus address 0x40



PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337, RE338 RE339, RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	



RE343	CE62	REV
* 240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4700p		
1K	4700p	

PD\_ACE\_DET# rise t1: nels measured from 5% to 68%

BOARD\_ID rise t1: nels measured from 5% to 68%

BOARD\_ID rise t1: nels measured from 5% to 68%

BOARD\_ID rise t1: nels measured from 5% to 68%

BOARD\_ID rise t1: nels measured from 5% to 68%

BOARD\_ID rise t1: nels measured from 5% to 68%

BOARD\_ID rise t1: nels measured from 5% to 68%

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BOARD\_ID rise t1: nels measured from 5% to 68%

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MECS105 Support

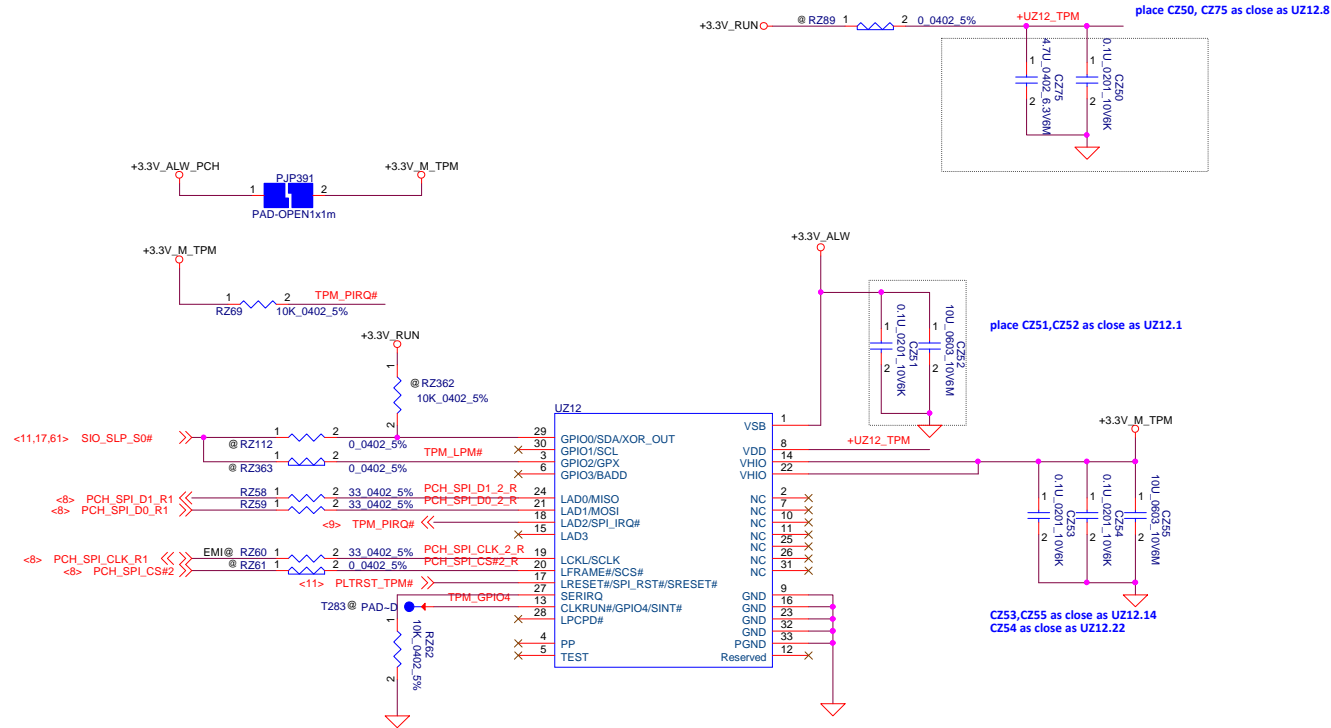
LA-E082P

Rev 1.0

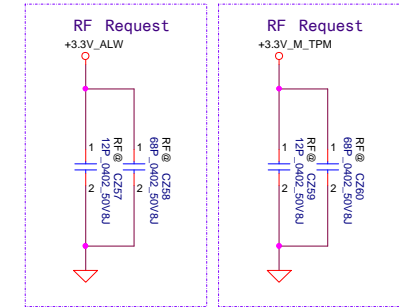
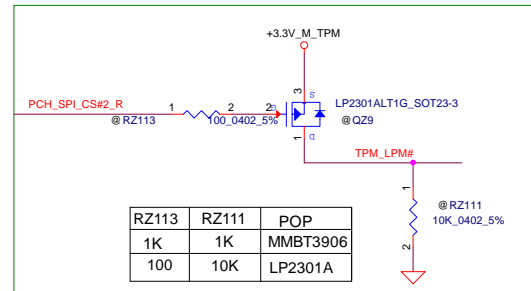
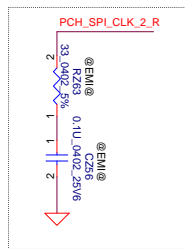
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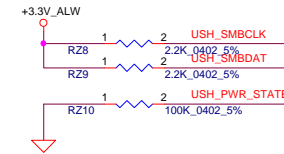
JB2YX change to VB2YX 09/08



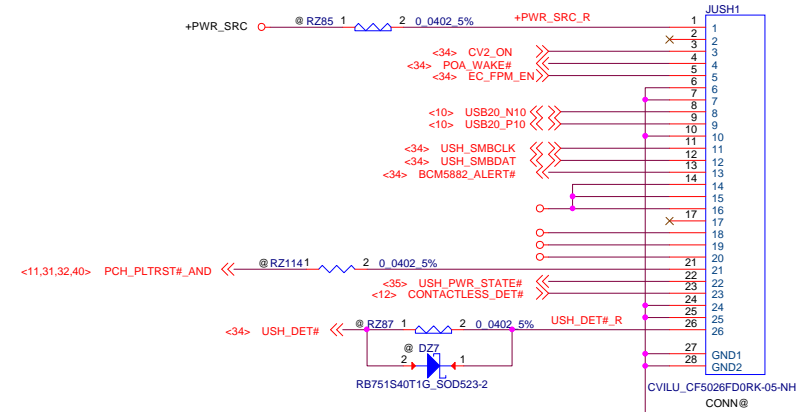
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Date: Monday, December 12, 2016		Sheet 36 of 75	

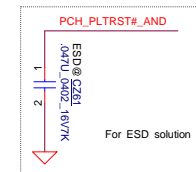
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USH CONN

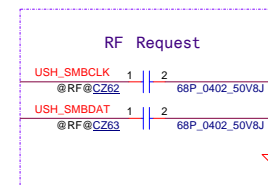
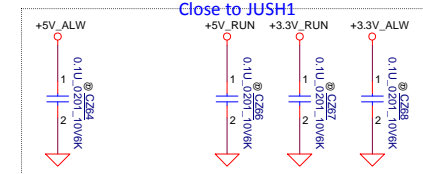


Link CVILU\_CF5026FD0RK-05-NH

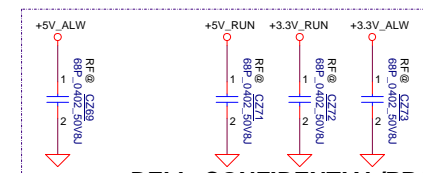


For ESD solution

Close to JUSH1



RF Request



RF Request

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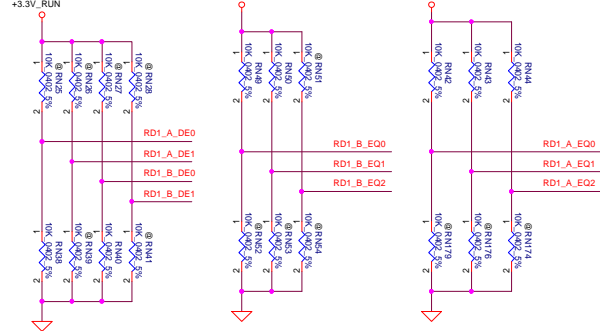
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Size	Document Number	Rev	
		1.0	
Date:	Monday, December 12, 2016	Sheet	37 of 75

vinafix

	PCIe/SATA Redriver for 2280
Brekenridge12	Need
Brekenridge14U UMA	Need
Brekenridge14U DSC	Need
Brekenridge15U UMA	Need
Brekenridge15U DSC	Need
Steamboat12	No need
Steamboat14	Need
Kirkwood12&13	Check

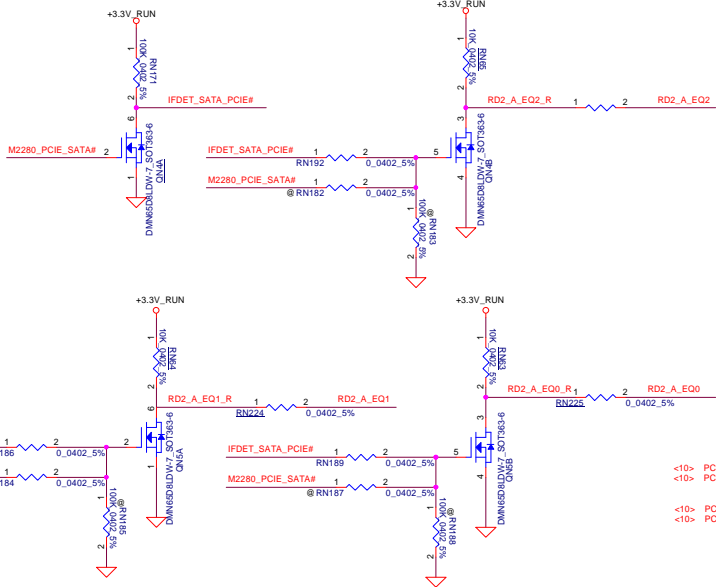
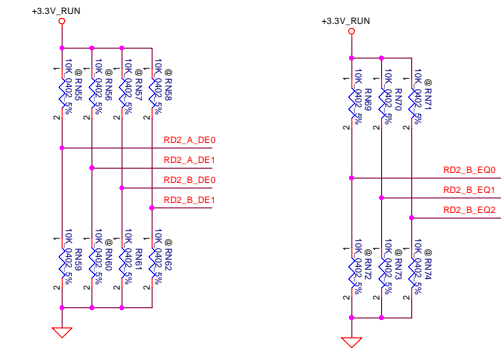


Programmable output de-emphasis level setting for channel A  
A\_DE0: internally pulled up at ~150K;  
A\_DE1 internally pulled down at ~150K  
[A\_DE1A\_DE0] ==  
LL: -20dB  
HL: -7.5dB  
LH: -3.5dB (default)  
HH: -6dB

Programmable output de-emphasis level setting for channel B  
B\_DE0: internally pulled up at ~150K;  
B\_DE1 internally pulled down at ~150K  
[B\_DE1B\_DE0] ==  
LL: -20dB  
HL: -7.5dB  
LH: -3.5dB (default)  
HH: -6dB

Equalizer control and program for channel A.  
A\_EQ0, A\_EQ1 and A\_EQ2: internally pulled down at ~150K  
[A\_EQ2A\_EQ1A\_EQ0] ==  
LLL: For channel loss up to 17dB (default)  
LHL: For channel loss up to 14dB  
HLL: For channel loss up to 19dB  
HHL: For channel loss up to 21dB  
LHH: For channel loss up to 18dB  
LHH: For channel loss up to 10dB  
HLH: For channel loss up to 16dB  
HHH: For channel loss up to 20dB

Equalizer control and program for channel B.  
B\_EQ0, B\_EQ1 and B\_EQ2: internally pulled down at ~150K  
[B\_EQ2B\_EQ1B\_EQ0] ==  
LLL: For channel loss up to 17dB (default)  
LHL: For channel loss up to 14dB  
HLL: For channel loss up to 19dB  
HHL: For channel loss up to 21dB  
LHH: For channel loss up to 18dB  
LHH: For channel loss up to 10dB  
HLH: For channel loss up to 16dB  
HHH: For channel loss up to 20dB

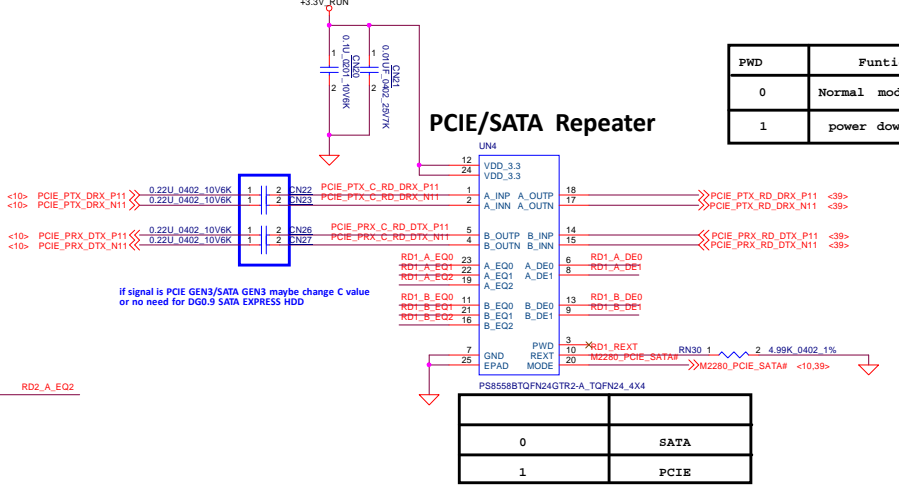


SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>

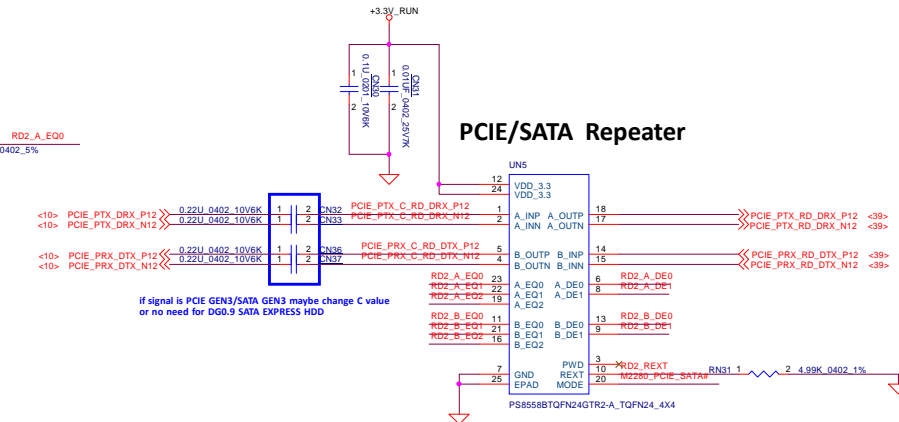
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PCIe/SATA Repeater



FWD	Function
0	Normal mode(default)
1	power down mode

PCIe/SATA Repeater



0	SATA
1	PCIe

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SATA/PCI REPEATER for M.2 2280

LA-E082P

Rev 1.0

For Breckenridge 14/15 DSC

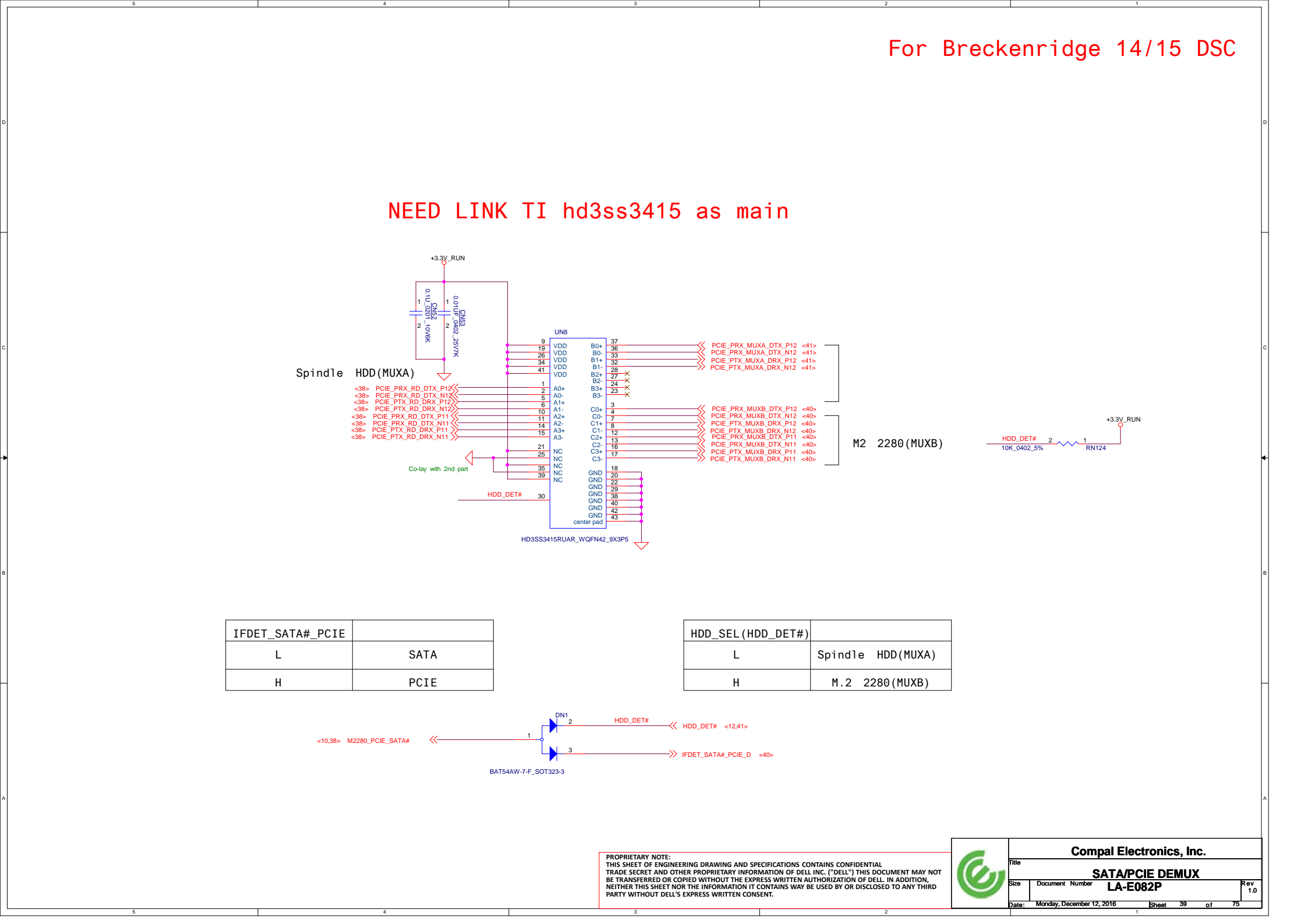
NEED LINK TI hd3ss3415 as main

IFDET_SATA#_PCIE	
L	SATA
H	PCIE

HDD_SEL(HDD_DET#)	
L	Spindle HDD(MUXA)
H	M.2 2280(MUXB)

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Size	Document Number	Rev	
	LA-E082P	1.0	
Date:	Monday, December 12, 2016	Sheet	39 of 75



For Breckenridge 14/15 DSC

NEED LINK TI hd3ss3415 as main

IFDET_SATA#_PCIE	
L	SATA
H	PCIE

HDD_SEL(HDD_DET#)	
L	Spindle HDD(MUXA)
H	M.2 2280(MUXB)

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	LA-E082P	1.0	
Date:	Monday, December 12, 2016	Sheet	39 of 75

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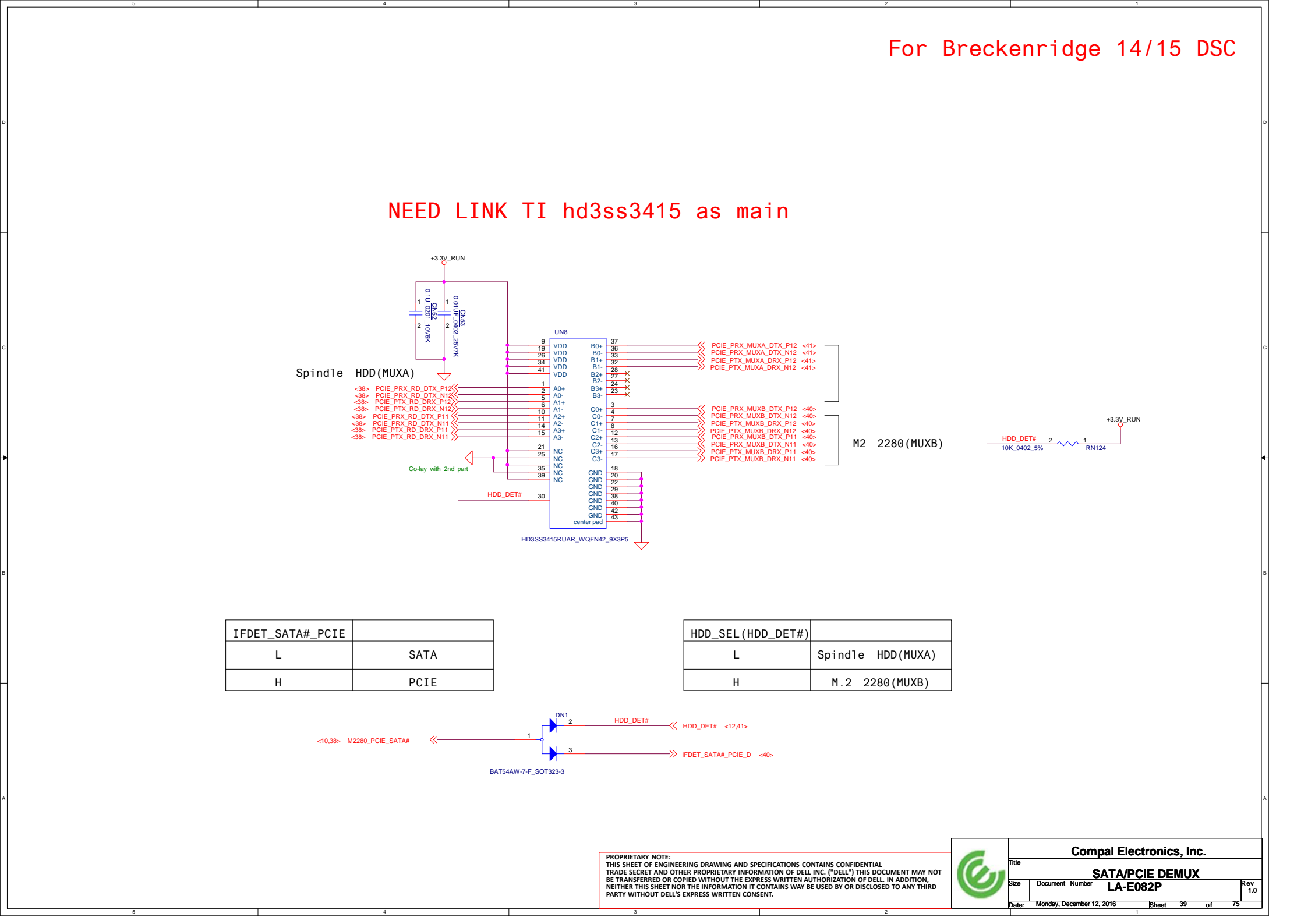
NEED LINK TI hd3ss3415 as main

IFDET_SATA#_PCIE	
L	SATA
H	PCIE

HDD_SEL(HDD_DET#)	
L	Spindle HDD(MUXA)
H	M.2 2280(MUXB)

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Date:	Monday, December 12, 2016	Sheet	39 of 75



For Breckenridge 14/15 DSC

NEED LINK TI hd3ss3415 as main

Schematic diagram showing the connection between a Spindle HDD(MUXA) and an M2 2280(MUXB) storage device via a UN8 connector.

The Spindle HDD(MUXA) is connected to the UN8 connector pins:

- VDD (Pins 9, 19, 26, 34, 41)
- A0+ (Pin 1), A0- (Pin 2), A1+ (Pin 5), A1- (Pin 10), A2+ (Pin 11), A2- (Pin 14), A3+ (Pin 15), A3- (Pin 15)
- NC (Pins 21, 25, 35, 39)
- GND (Pins 18, 20, 22, 29, 38, 40, 42, 43)
- HDD\_DET# (Pin 30)

The M2 2280(MUXB) is connected to the UN8 connector pins:

- B0+ (Pin 37), B0- (Pin 36), B1+ (Pin 33), B1- (Pin 32), B2+ (Pin 28), B2- (Pin 27), B3+ (Pin 24), B3- (Pin 23)
- C0+ (Pin 3), C0- (Pin 4), C1+ (Pin 7), C1- (Pin 8), C2+ (Pin 12), C2- (Pin 13), C3+ (Pin 16), C3- (Pin 17)
- NC (Pins 18, 20, 22, 29, 38, 40, 42, 43)
- GND (Pins 18, 20, 22, 29, 38, 40, 42, 43)

Power supply connections include +3.3V\_RUN and GND. The HDD\_DET# signal is connected to the HDD\_DET# pin of the M2 2280(MUXB).

Additional components shown include capacitors (0.1µF, 0.047µF, 100nF) and resistors (RN124).

IFDET_SATA#_PCIE	
L	SATA
H	PCIE

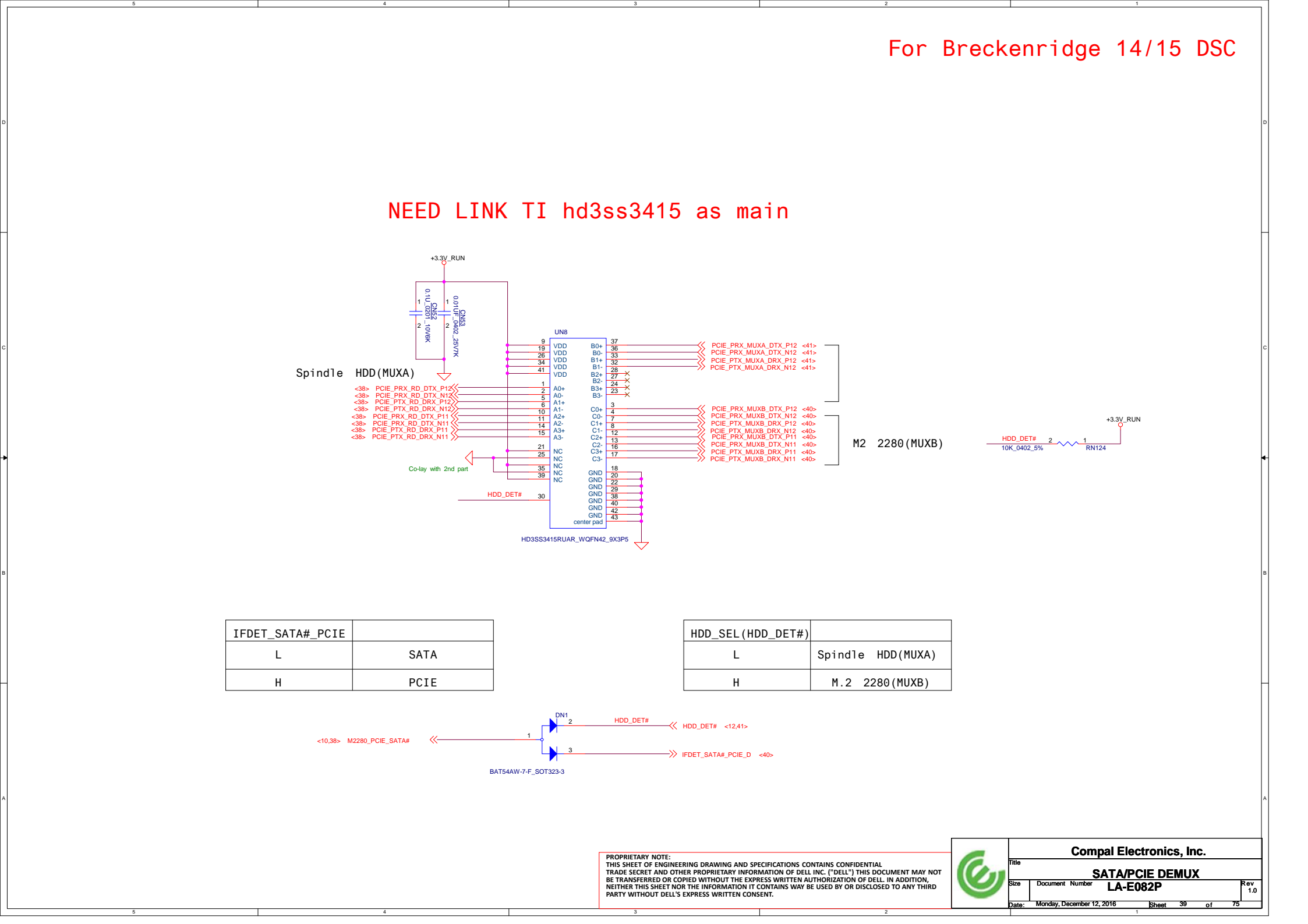
HDD_SEL (HDD_DET#)	
L	Spindle HDD(MUXA)
H	M.2 2280(MUXB)

Schematic diagram showing the connection between the IFDET\_SATA#\_PCIE signal and the HDD\_DET# signal.

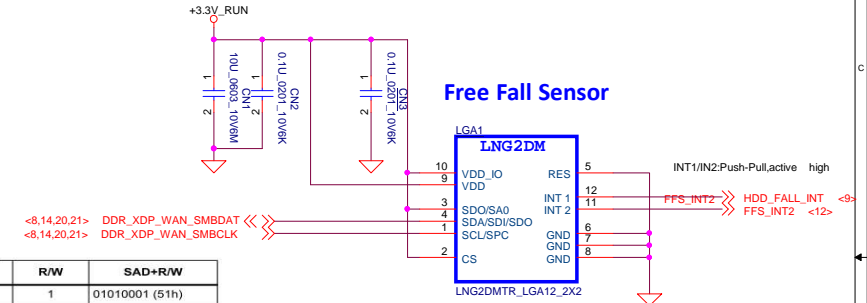
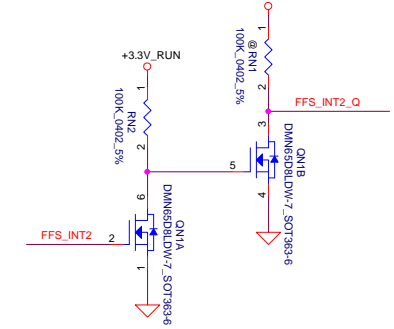
The IFDET\_SATA#\_PCIE signal is connected to the DN1 pin of the BAT54AW-7-F\_SOT323-3 diode. The output of the diode is connected to the HDD\_DET# signal.

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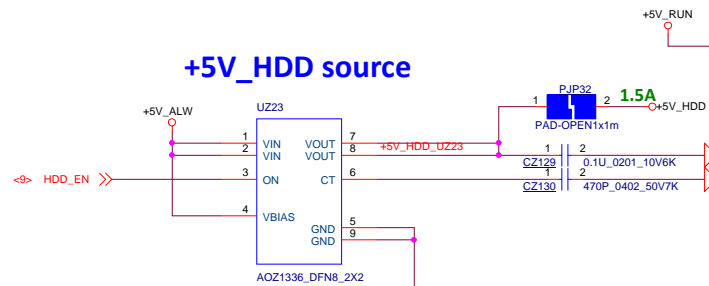
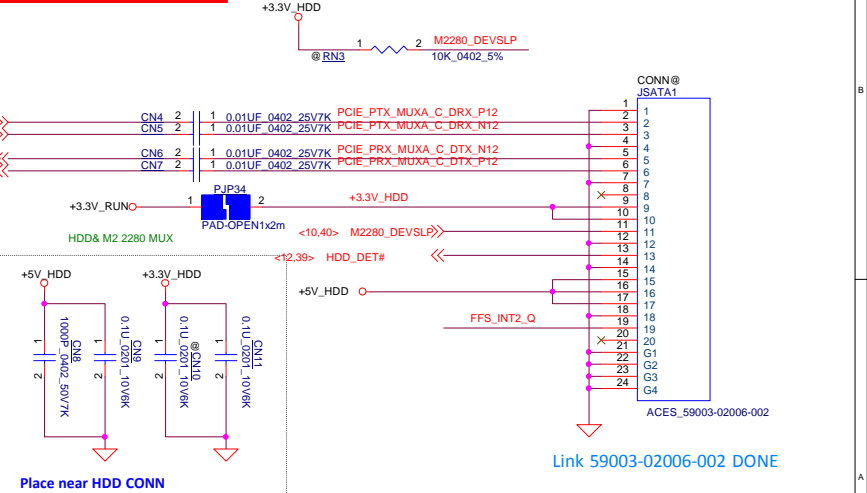
Title			
SATA/PCIE DEMUX			
Size	Document Number	Rev	
	LA-E082P	1.0	
Date:	Monday, December 12, 2016	Sheet	39 of 75



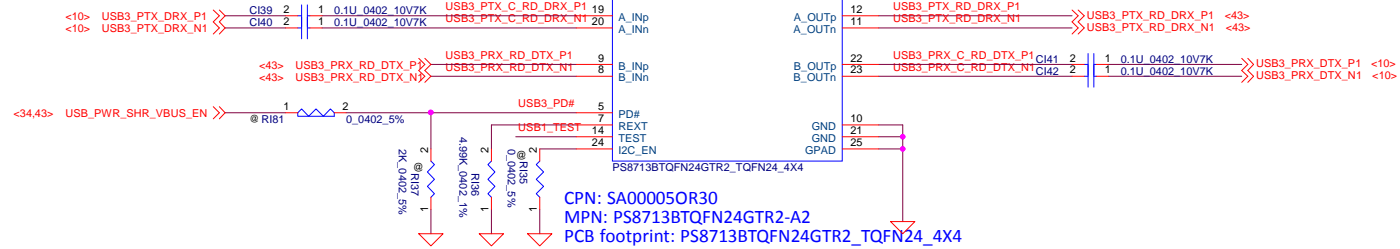
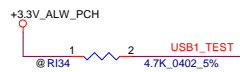
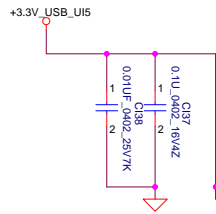
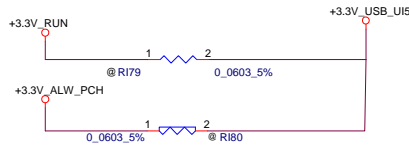




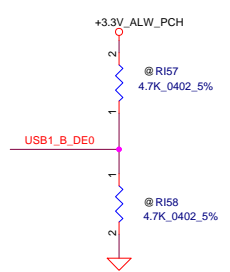
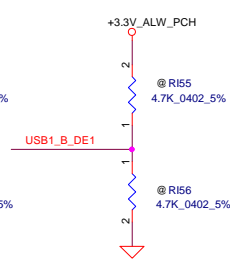
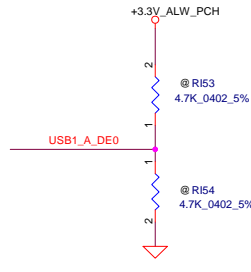
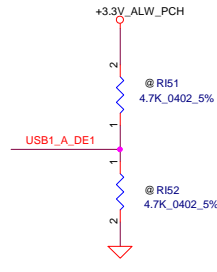
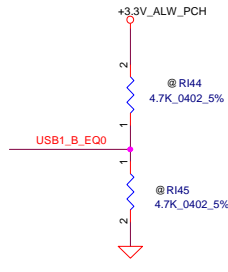
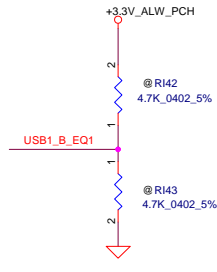
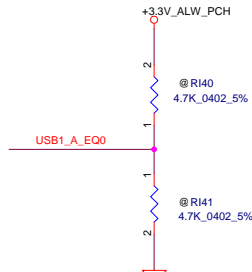
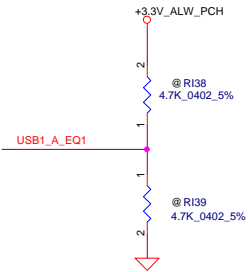
Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)



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	USB3 Redriver for charge
Brekenridge12	No need
Brekenridge14U UMA	Need
Brekenridge14U DSC	Need
Brekenridge15U UMA	Need
Brekenridge15U DSC	Need
Steamboat12	Need
Steamboat14	Need
Kirkwood12&13	Check



### Parade\_PS8713B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 13dB
1	0	1	0	loss up to 4.5dB
1	1	1	1	loss up to 7.5dB

A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	3.5dB de-emphasis
0	1	0	1	No de-emphasis
1	0	1	0	2.7dB de-emphasis
1	1	1	1	5dB de-emphasis

Both A\_EQ&B\_EQ have internal pull-down 150k

Both A\_DE&B\_DE have internal pull-down 150k

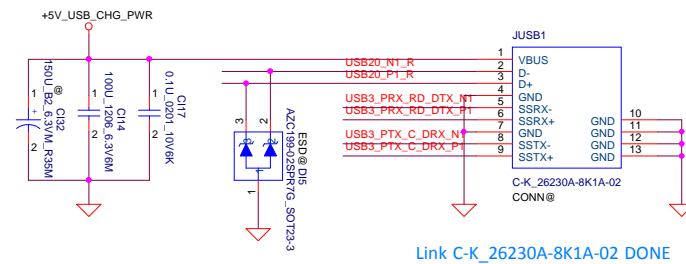
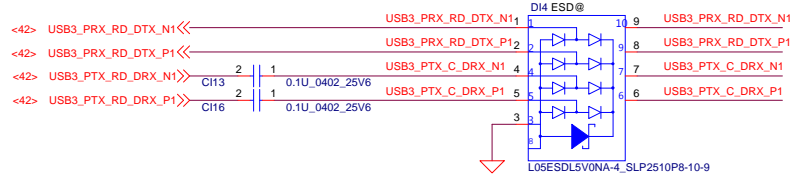
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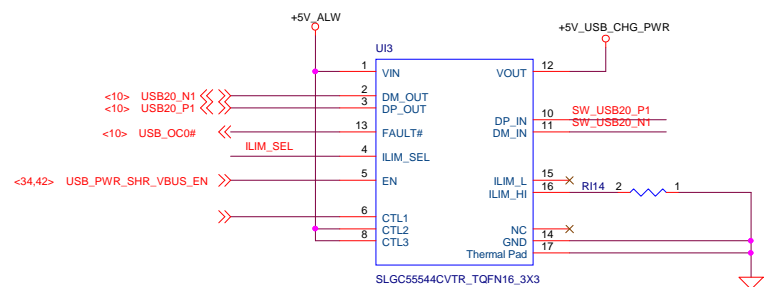
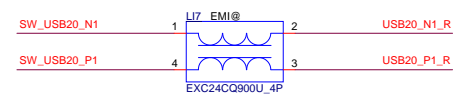


Compal Electronics, Inc.		
Title		
USB3.0 Repeater		
Size	Document Number	Rev
	LA-E082P	1.0
Date:	Monday, December 12, 2016	
Sheet	42	of 75

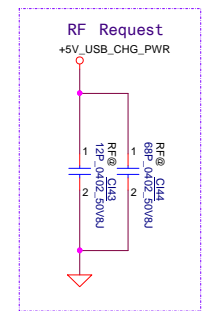
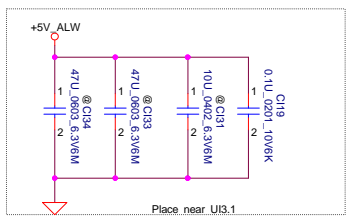
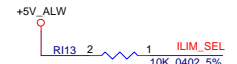
For w/ Repeater



Link C-K\_26230A-8K1A-02 DONE



Link Seligro SA000097E10 Done  
MAIN:SLGC55544CVTR

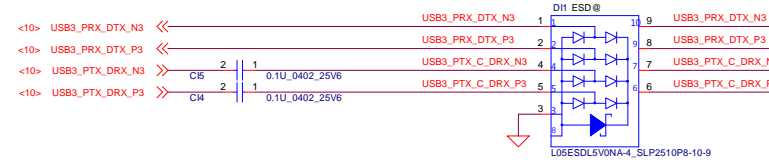


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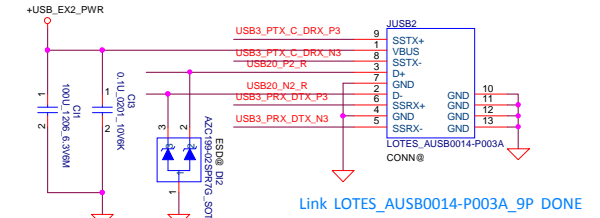
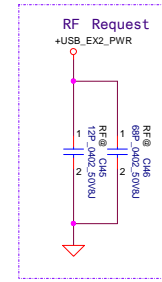
Compal Electronics, Inc.			
Title			
JUSB1+PS			
Size	Document Number	Rev	
	LA-E082P	1.0	
Date:	Monday, December 12, 2016	Sheet	43 of 75

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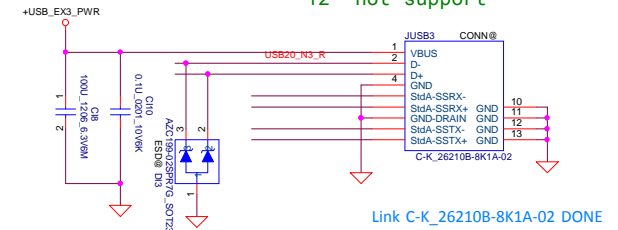
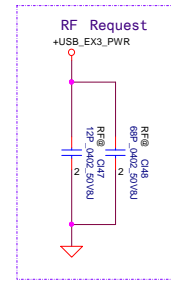
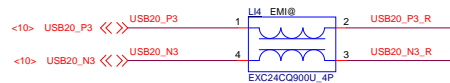
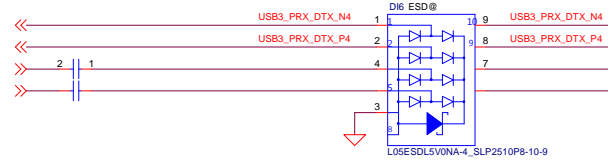
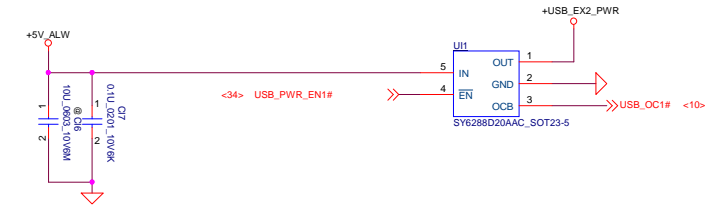
# For Breckenridge 14&15/Steamboat 14



DfB request:  
main SM070003200 (INPAQ\_MCM1012B900F06BP\_4P)  
Footprint use 2nd source SM070004400 (PANAS\_EXC24CQ900U\_4P)  
Pitch change from 0.5mm to 0.55mm

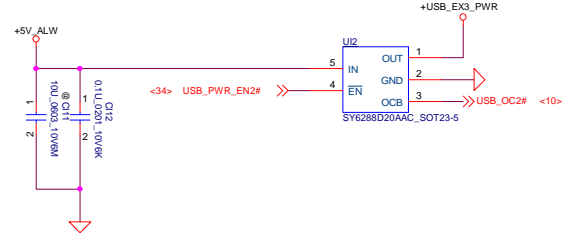


Link LOTES\_AUSB0014-P003A\_9P DONE



12" not support

Link C-K\_26210B-8K1A-02 DONE



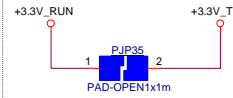
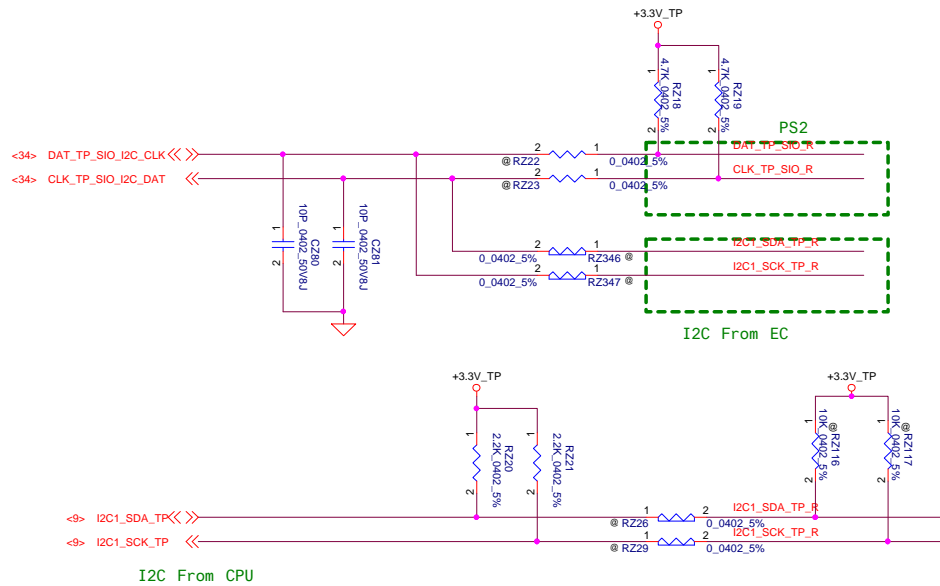
**vinafix**

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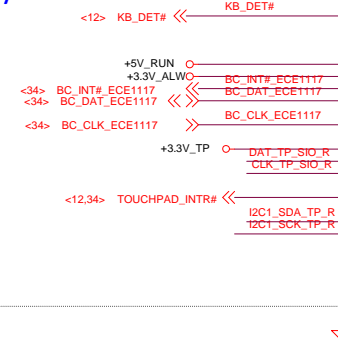
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JUSB2&JUSB3	
LA-E082P	Rev 1.0
Date: Monday, December 12, 2016	Sheet 44 of 75

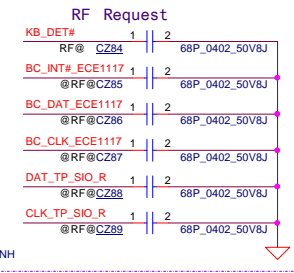
## Touch Pad



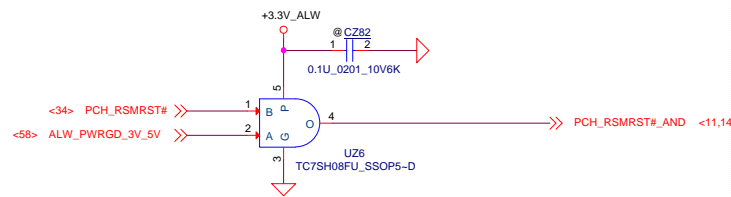
## Keyboard



Link HRS\_TF49-20S-0P5SH done



## RSMRST circuit



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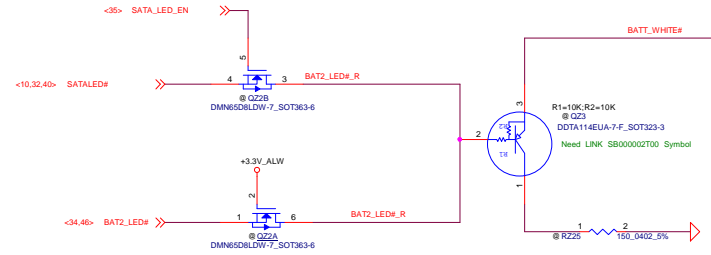
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Compal Electronics, Inc.			
Title			
Keyboard			
Size	Document Number	Rev 1.0	
Date: Monday, December 12, 2016		Sheet 45	of 75

## Battery LED

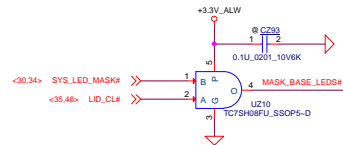
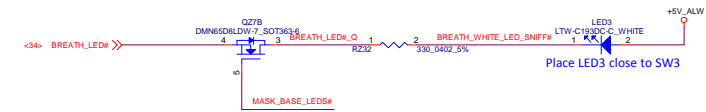
### HDD LED MUX

means EC can switch battery white led and HDD LED by hot key - Fn+F1

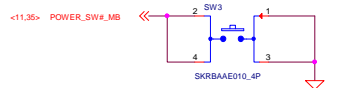


## Breath LED

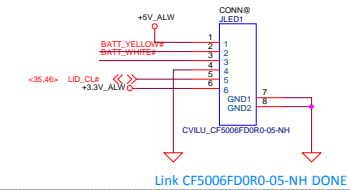
LED PIN change to SC50000FL00 from SC50000BA00



### POWER & INSTANT ON SWITCH



### LED board CONN

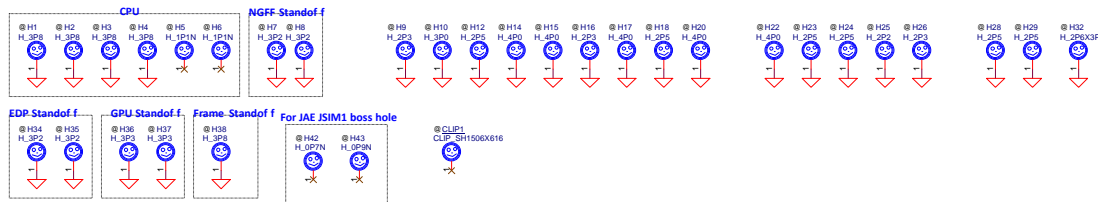


### Fiducial Mark



### LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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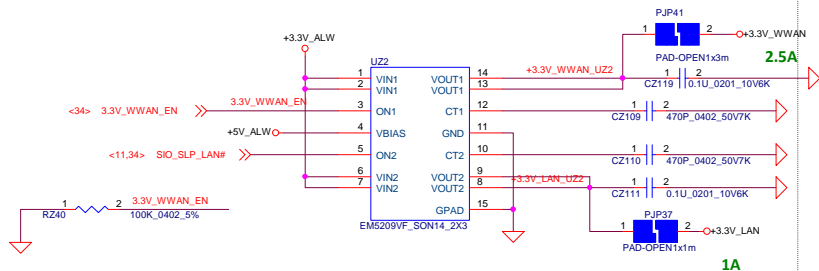
Compal Electronics, Inc.



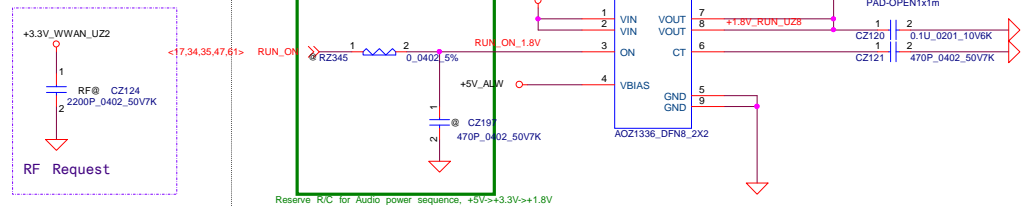
Rev	1.0
Size	Document Number
Date	Monday, December 12, 2016
Sheet	46 of 75

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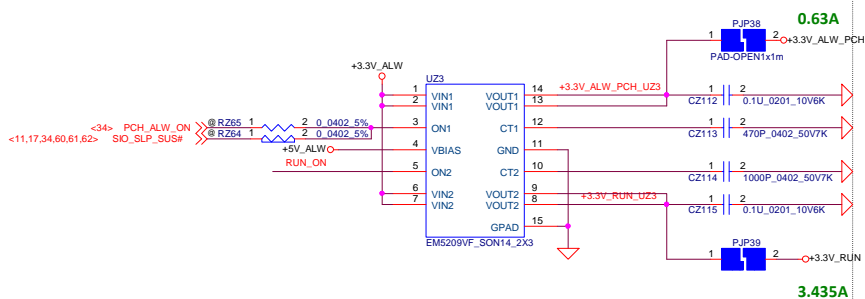
### +3.3V\_WWAN/+3.3V\_LAN source



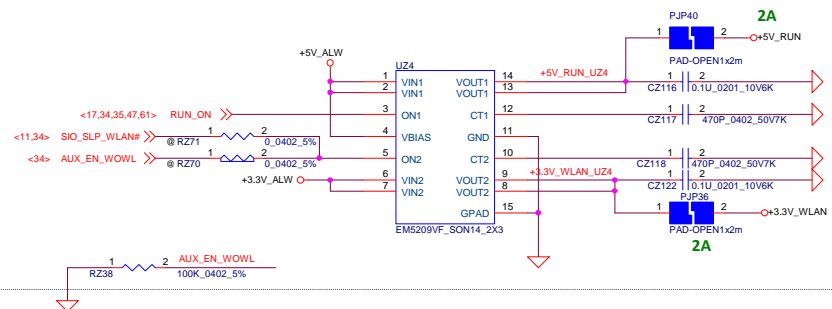
### +1.8V\_RUN source



### +3.3V\_ALW\_PCH/+3.3V\_RUN source



### +5V\_RUN/+3.3V\_WLAN source



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Power control

LA-E082P

Date: Monday, December 12, 2016 Sheet 47 of 75

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I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E(Default)
1	0x9C(Multi-GPU usage)

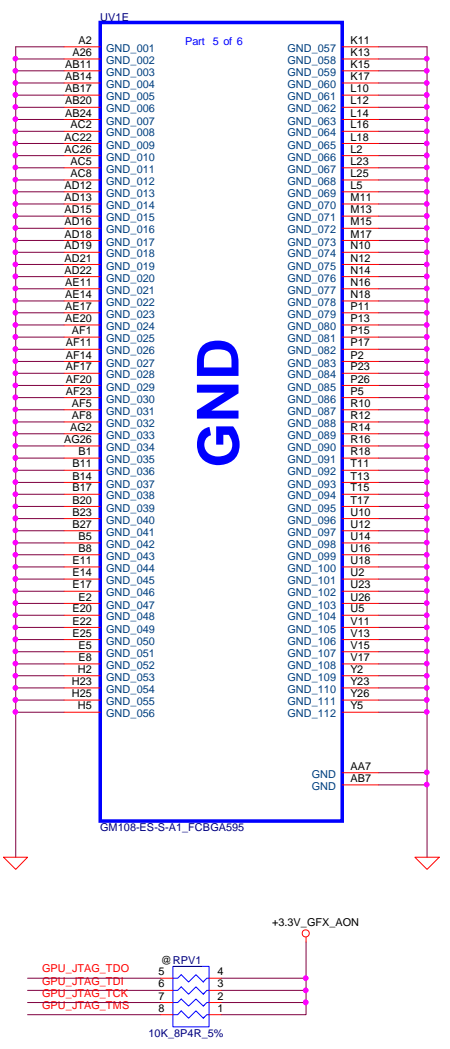
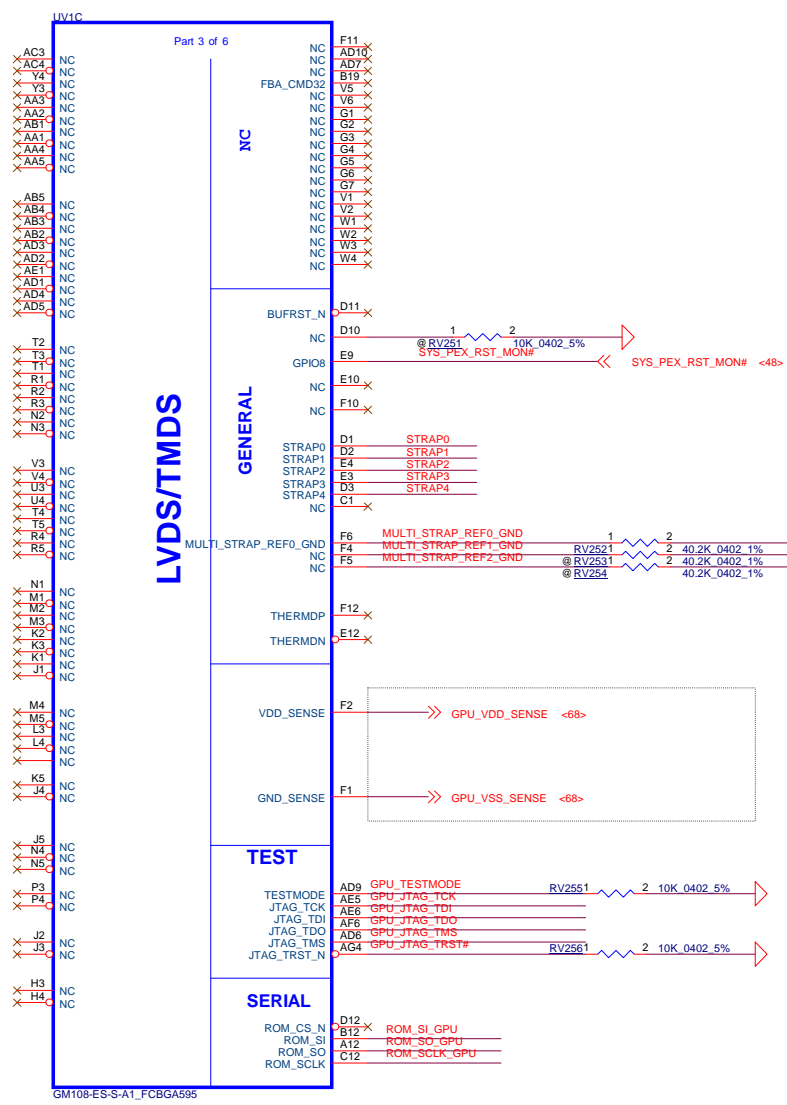
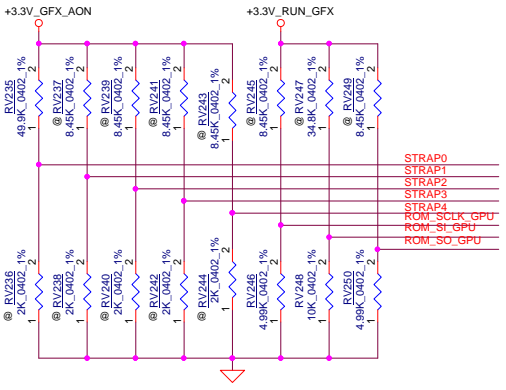
VGA\_DEVICE Setting

VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device(Class Code 302h)
1	Primary Display or VGA Device(Class Code 300h)

Resistance Mapping to Hex Values

Resistor Value	Pull-up to VDD33	Pull-down to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111


Decive ID change to 0x1056



Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0	Note
ROM_SCLK	SOR3_EXPOSED->0	SOR2_EXPOSED->0	SOR1_EXPOSED->0	SOR0_EXPOSED->0	ROM_SCLK pull-down RV246 4.99k to GND
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	ROM_SI pull-down RV248 24.9k to GND
ROM_SO	DEVID_SEL->0(default)	PCIE_CFG->0(default)	SMB_ALT_ADDR->0(default)	VGA_DEVICE->0	ROM_SO pull-down RV250 4.99k to GND
STRAP0	Keep pull up to 3V3_AON and pull-down to GND footprint and stuff 50k ohm pull up				STRAP0 pull up RV235 50k to +3.3V_GFX_AON
STRAP1 STRAP2 STRAP3 STRAP4	Reserve				

DEVID\_SEL/PCIE\_CFG default set 0, need refer Platform Update Notification for the latest configuration

VENDER	STRAP	Part Number	Note(ROM_SI)
Hynix	0x7	H5TC4G63CFR-N0C	RV248 45.3K PD
Micron	0x6	MT41J256M16LY-091G:N	RV248 34.8K PD
Samsung	0x1	K4W4G1646E-BC1A	RV248 10k PD



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**N15S DP, STRAP, GND**

**LA-E082P**

Monday, December 12, 2016

Size

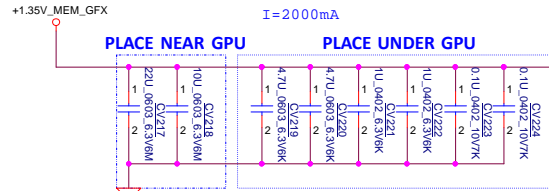
Document Number

Date

Rev 1.0

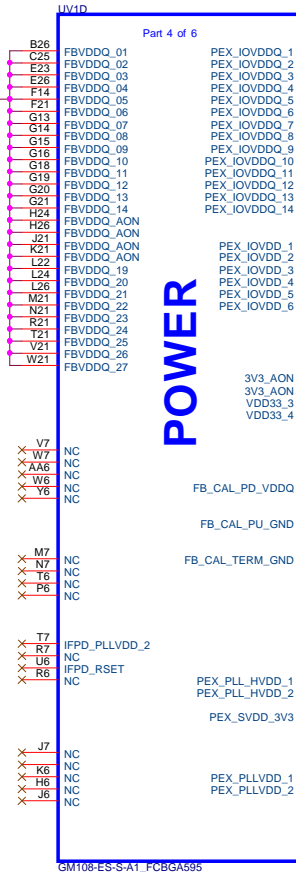
Sheet 49 of 75

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DDR3 CPU side FBVDD/FBVDDQ Combined Decoupling		
Capacitor Type	Population	
0.1uF 0402	2	
1.0uF 0603	2	
4.7uF 0603	2	
10uF 0805	1	
22uF 0805	1	

Power Supply Rail	N16S-GMR	
	(V)	(A)
GPU_Core	-	21
GPU_FBIO	1.5/1.35	1.4
PEX_IOVDD/Q	1.0	
PEX_PLLVDD	1.0	
FBA_PLL_AVDD	1.0	
FBA_DLL_AVDD	1.0	
PLL_VDD	1.0	
SP_PLLVDD	1.0	
<b>1.1V Total</b>	1.0	0.8
VDD33+3V3AON	3.3	
PEX_SVDD_3V3	3.3	
PEX_PLL_HVDD	3.3	
<b>3.3V Total</b>	3.3	0.06



POWER

PEX_PLLVDD Decoupling		
Capacitor Type	Population	
0.1uF 0402	1	
1uF 0603	1	
4.7uF 0805	1	

PEX_SVDD/PEX_PLL_HVDD Decoupling		
Capacitor Type	Population	
0.1uF 0402	1	
4.7uF 0603	2	

3V3_MAIN Decoupling		
Capacitor Type	Population	
0.1uF 0402	2	
1uF 0603	1	
4.7uF 0603	1	

3V3_AON Decoupling		
Capacitor Type	Population	
0.1uF 0402	1	
1uF 0603	1	
4.7uF 0603	1	

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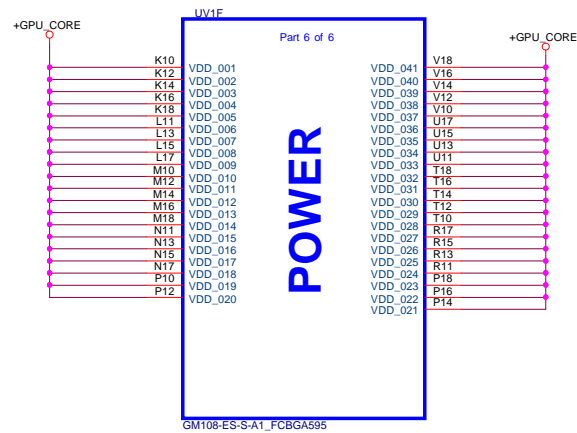


N15S Power			
Size	Document Number	Rev	
	LA-E082P	1.0	
Date:	Monday, December 12, 2016	Sheet	50 of 75

vinafix

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Caps on Power Side  
1UX4 4.7UX10 under GPU  
4.7UX5 22UX1 47UX2 330UX2 near GPU



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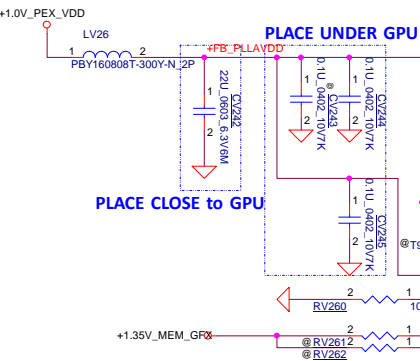


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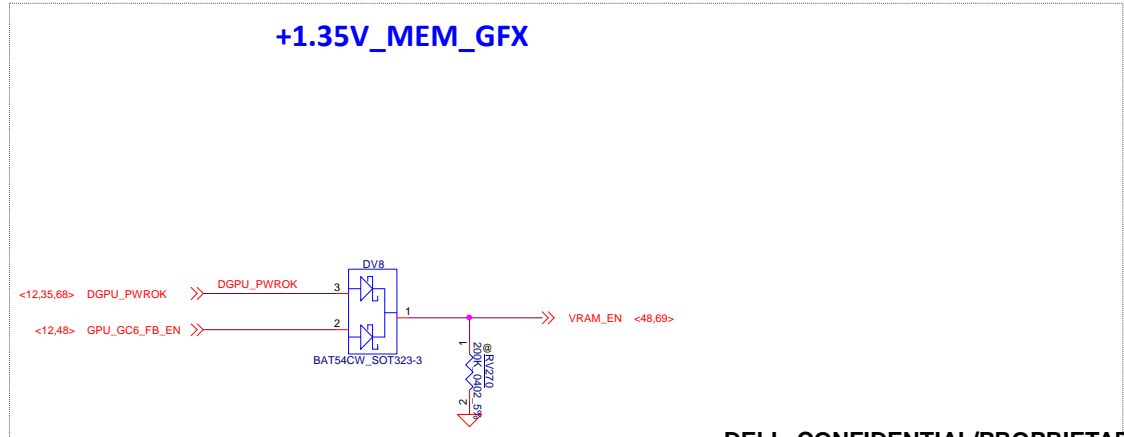
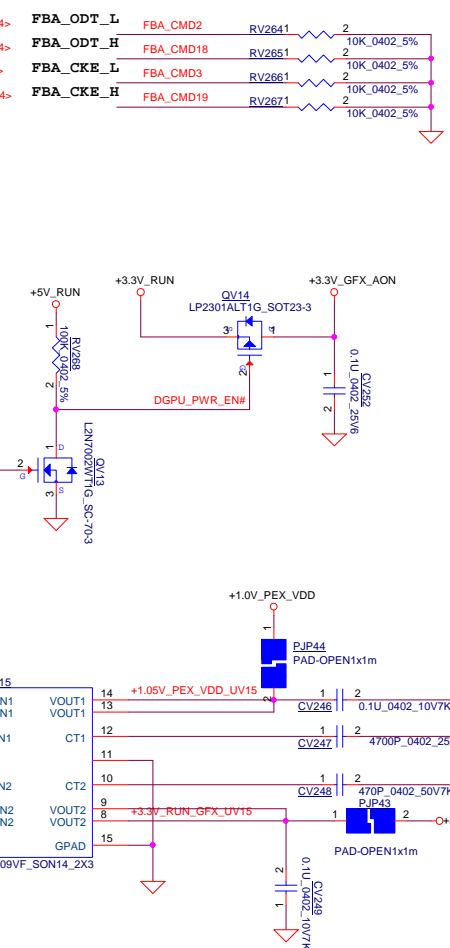
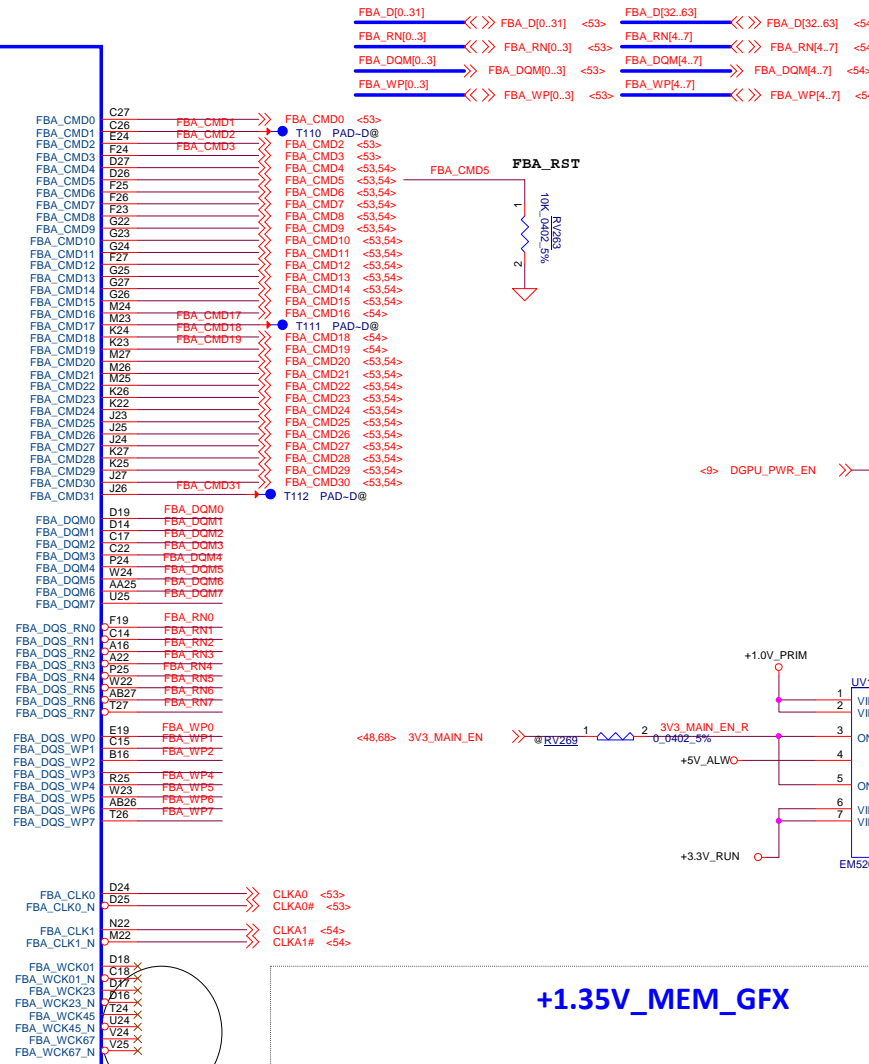
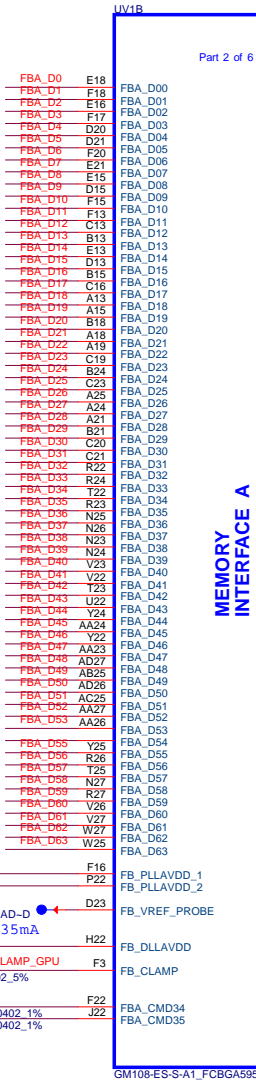
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Title		N15S Power GFX Core	
Size	Document Number	Rev	
	LA-E082P	1.0	
Date:	Monday, December 12, 2016	Sheet	51 of 76

CMD0	CS0#	CMD32	
CMD1		CMD33	
CMD2	ODT	CMD34	
CMD3	CKE	CMD35	
CMD4	A14	CMD36	A14
CMD5	RST	CMD37	RST
CMD6	A7	CMD38	A7
CMD7	A2	CMD39	A7
CMD8	A2	CMD40	A2
CMD9	A0	CMD41	A0
CMD10	A4	CMD42	A4
CMD11	A0	CMD43	A1
CMD12	BA0	CMD44	BA0
CMD13	WE#	CMD45	WE#
CMD14	A15	CMD46	A15
CMD15	CS#	CMD47	CS#
CMD16		CMD48	CS0#
CMD17		CMD49	
CMD18		CMD50	ODT
CMD19		CMD51	CKE
CMD20	A13	CMD52	A13
CMD21	A8	CMD53	A8
CMD22	A0	CMD54	A0
CMD23	A11	CMD55	A11
CMD24	A5	CMD56	A5
CMD25	A3	CMD57	A3
CMD26	BA2	CMD58	BA2
CMD27	BA1	CMD59	BA1
CMD28	A12	CMD60	A12
CMD29	A10	CMD61	A10
CMD30	RAS#	CMD62	RAS#
CMD31		CMD63	



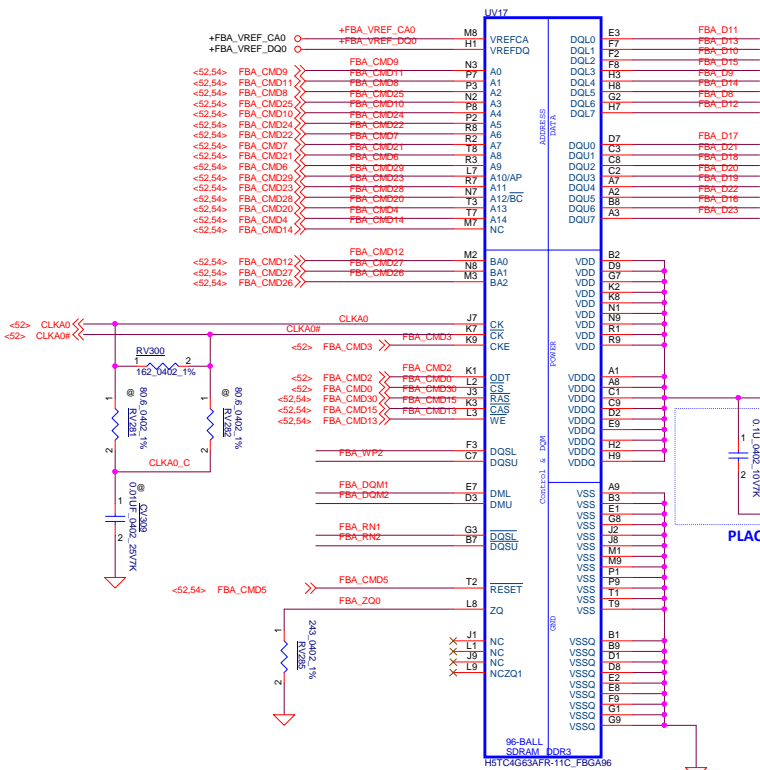
FBx_PLL_AVDD and FB_DLL_AVDD Combined	
Capacitor Type	Population
0.1uF 0402	2
22uF 0805	1
Bead 30 ohm (ESR=0.01 ohm) 0603	1



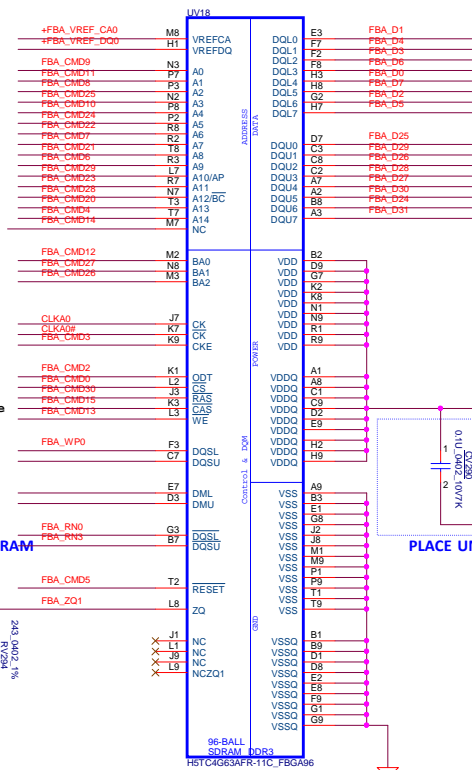
	<b>Compal Electronics, Inc.</b>		
	Title		
	<b>N15S Memory</b>		
	Size	Document Number	Rev
	<b>LA-E082P</b>		<b>1.0</b>
Date:	Monday, December 12, 2016		Sheet 52 of 75

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FBA\_D[0..31] <<> FBA\_D[0..31] <52>  
 FBA\_WP[0..3] <<> FBA\_WP[0..3] <52>  
 FBA\_DOM[0..3] <<> FBA\_DOM[0..3] <52>  
 FBA\_RN[0..3] <<> FBA\_RN[0..3] <52>

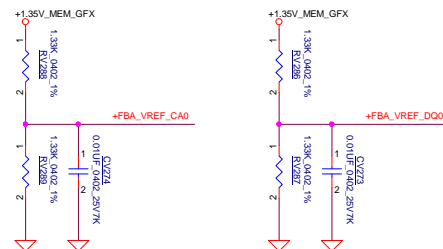


SA00006E800 Link done



SA00006E800 Link done

DDR3 per Memory FBVDD/Q Decoupling	
FBVDD/Q Combined	
Capacitor Type	Population
0.1uF 0402	2
1.0uF 0603	4
10uF 0805	0

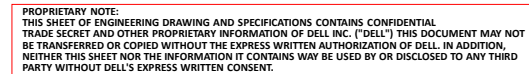
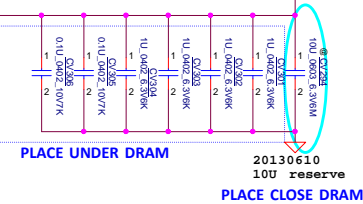
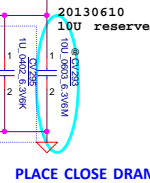


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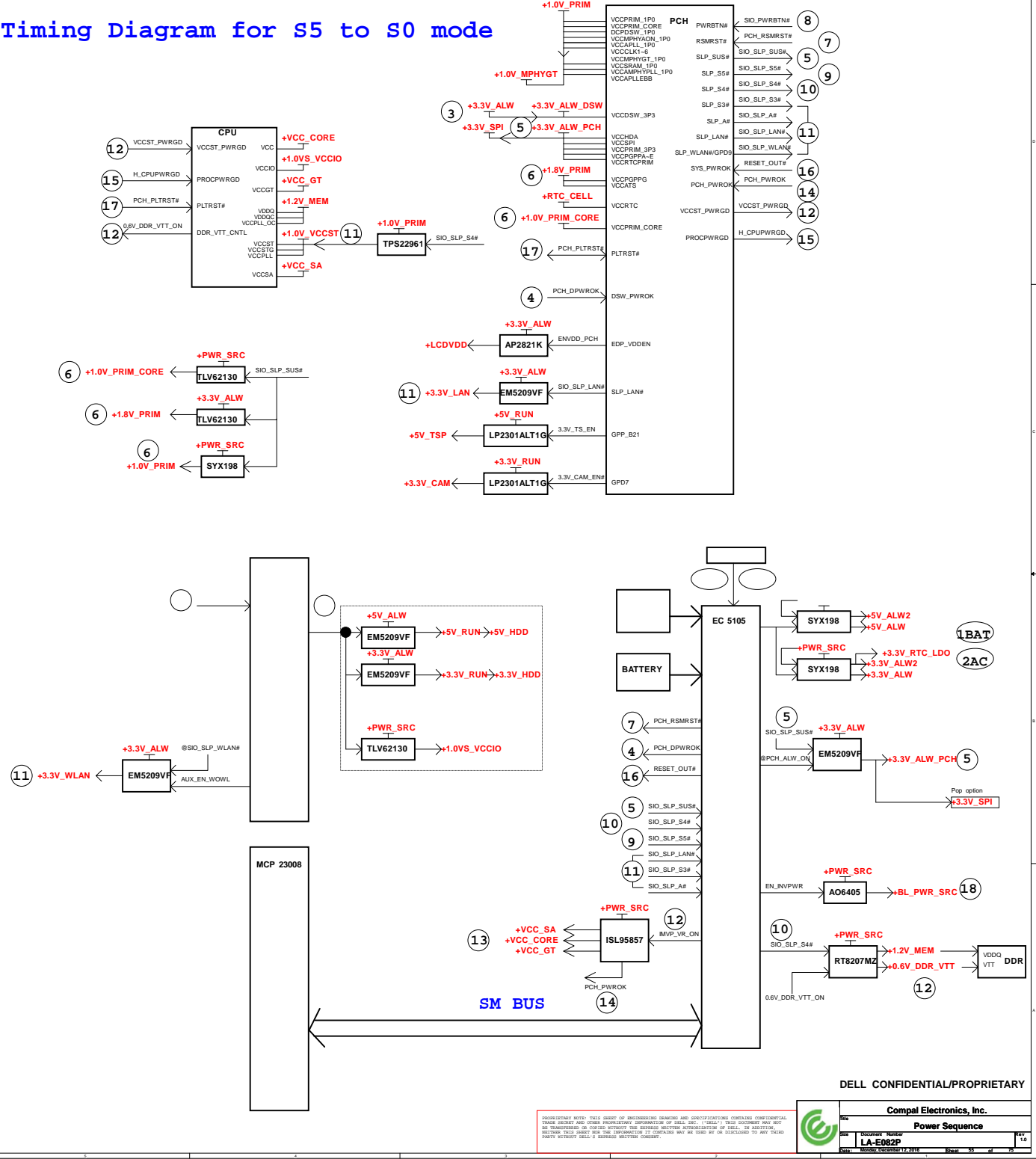
Compal Electronics, Inc.			
Title	MARX-VRAM A Lower		
Size	Document Number	Rev	
	LA-E082P	1.0	
Date:	Monday, December 12, 2016	Sheet	53 of 75

256x16 DDR3L



Title				MARX-VRAM_A Lower				Rev	
Size		Document Number						1.	
		LA-E082P							
Date: Monday, December 12, 2016				Sheet 54		of 75			

Timing Diagram for S5 to S0 mode



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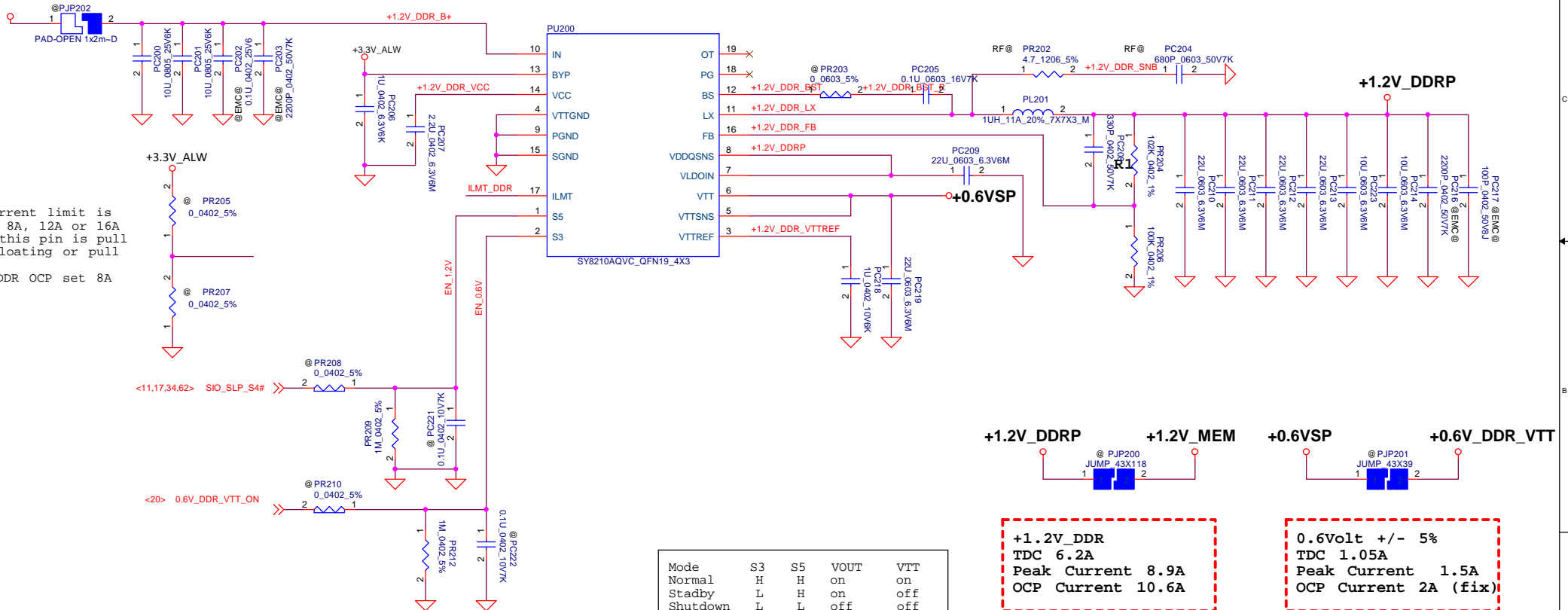






# vinafix

## +PWR\_SRC



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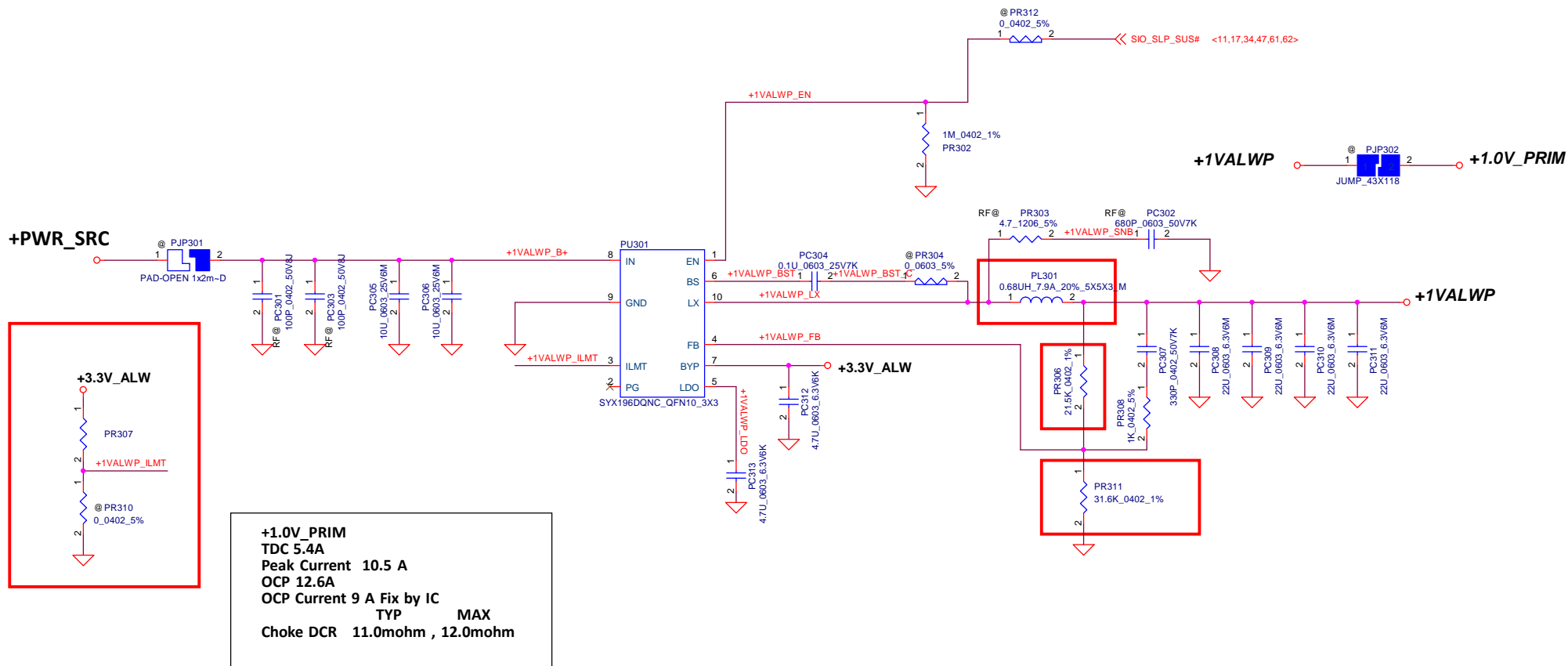
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Title  
**+1.2V\_MEN/+0.6V\_DDR\_VTT**

Size      Document Number      Rev  
**LA-E082P**      0.1

Date: Monday, December 12, 2016      Sheet 59 of 71

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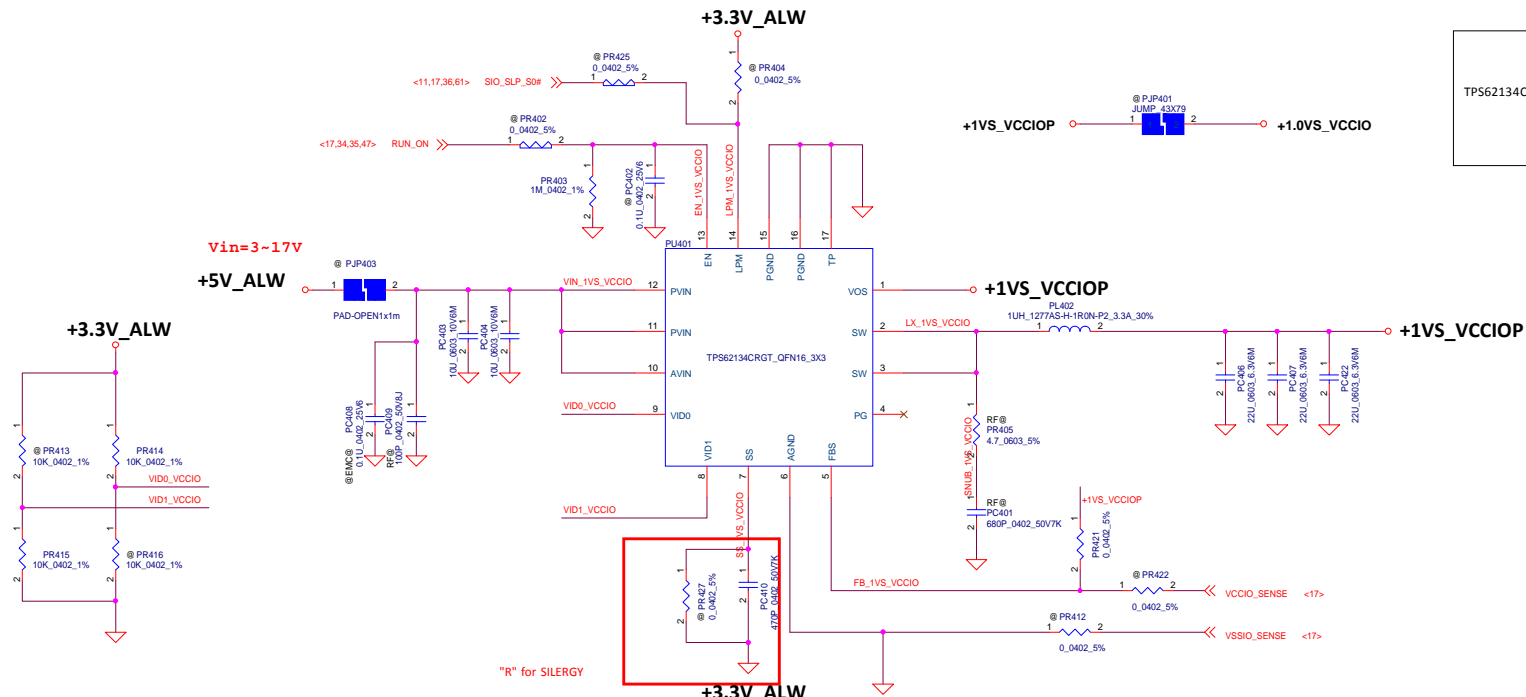


The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

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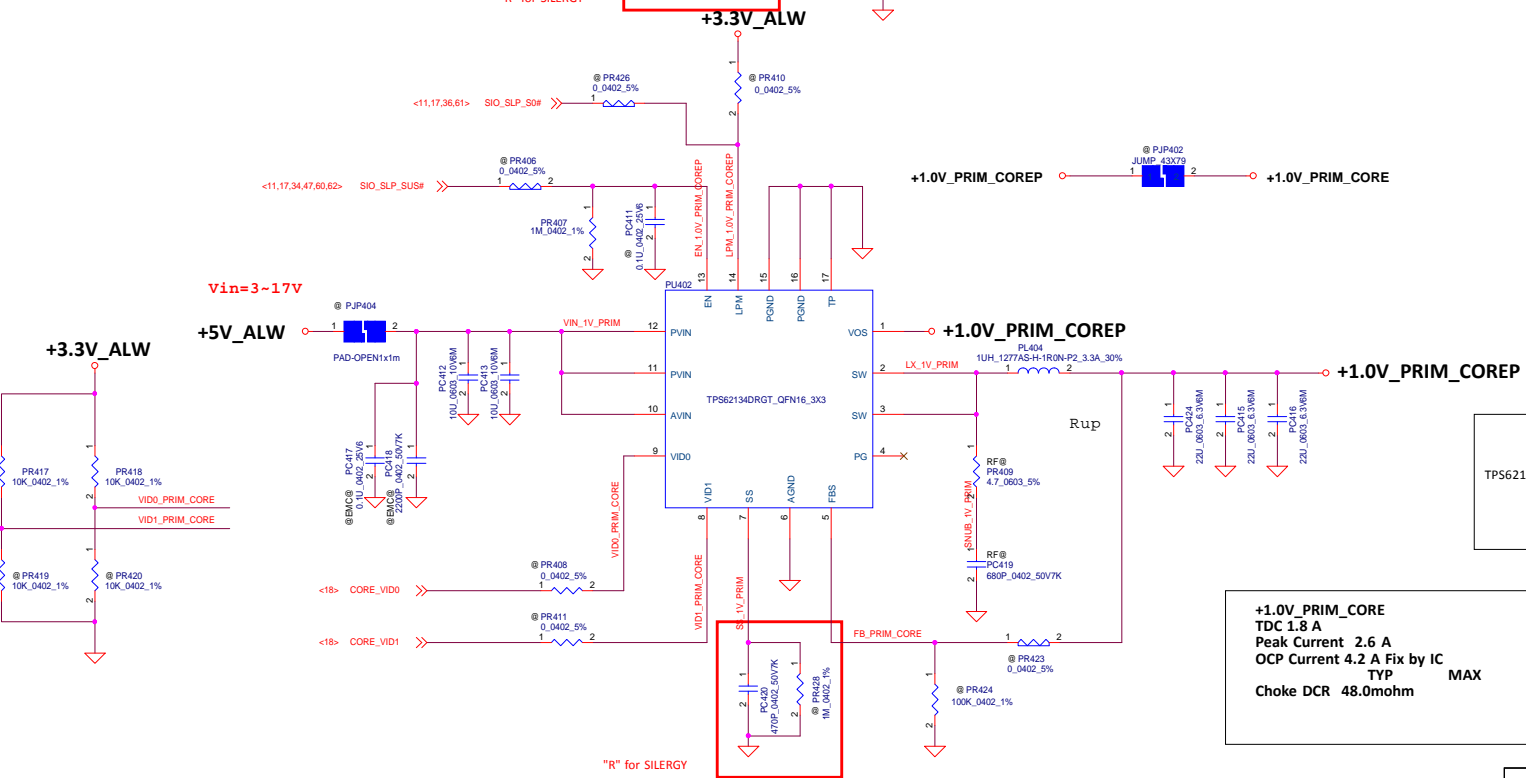
Compal Electronics, Inc.		
Title		
+1VALWP		
Size	Document Number	Rev
	LA-E082P	0.1
Date:	Monday, December 12, 2016	Sheet 60 of 71

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	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
TPS62134C	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

**+1.0VS\_VCCIO**  
**TDC 2.2 A**  
**Peak Current 3.1 A**  
**OCF Current 4.2 A Fix by IC**  
**TYP**  
**Choke DCR 48.0mohm**  
**MAX**



	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
TPS62134D	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

**+1.0V\_PRIM\_CORE**  
**TDC 1.8 A**  
**Peak Current 2.6 A**  
**OCF Current 4.2 A Fix by IC**  
**TYP**  
**Choke DCR 48.0mohm**  
**MAX**

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Local sense put on HW site

+1.0V\_VCCST

VCC\_SA  
TDC 4A  
Peak Current 4.5A  
OCP current 5.4A  
Choke DCR 13 m ohm

VCCSA\_B+  
CPU\_B+  
PAD-OPEN1x1m

VCCSA\_B+

+VCC\_SA

+5V\_ALW

+5V\_ALW

+3.3V\_RUN

<15> VCCSENSE

<15> VSSSENSE

Local sense put on HW site

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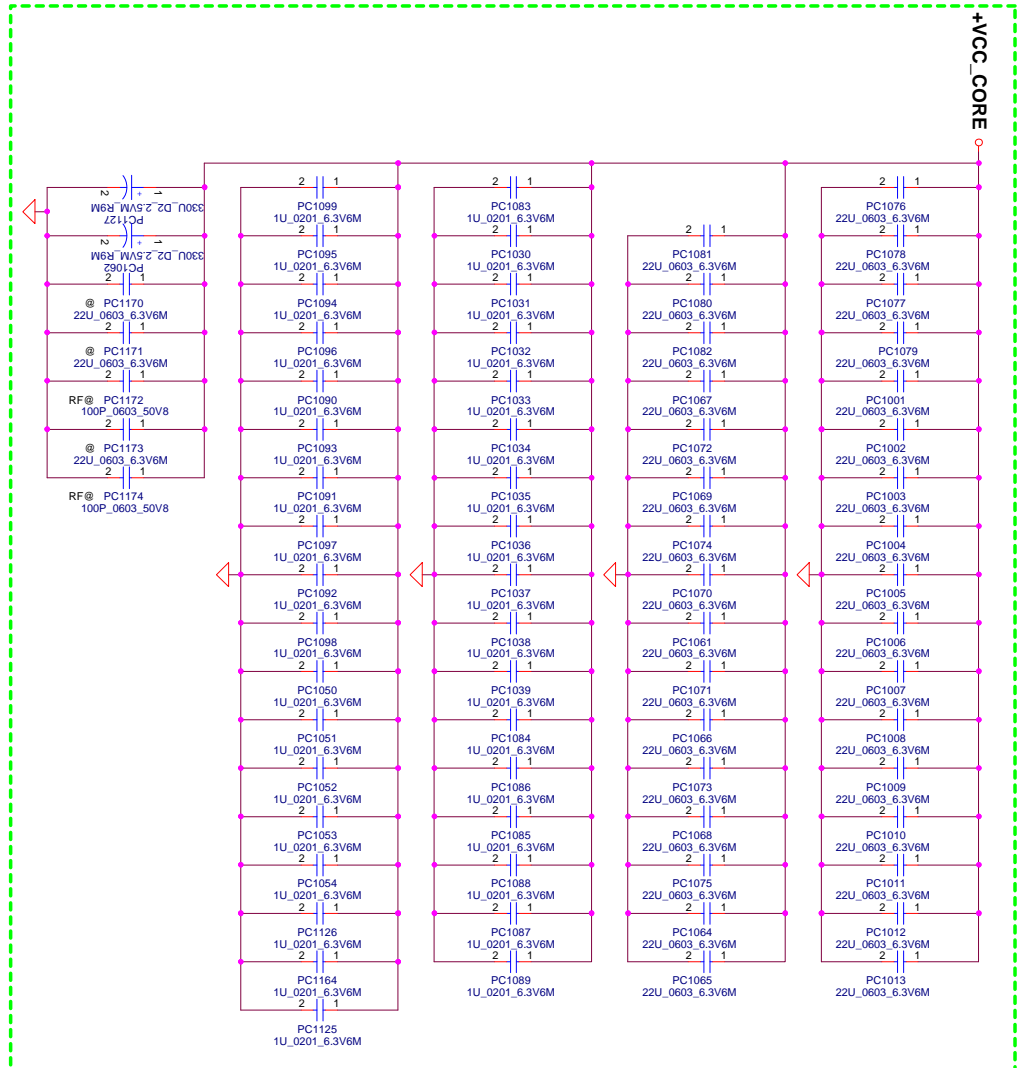
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VCCSA\_ISL95857

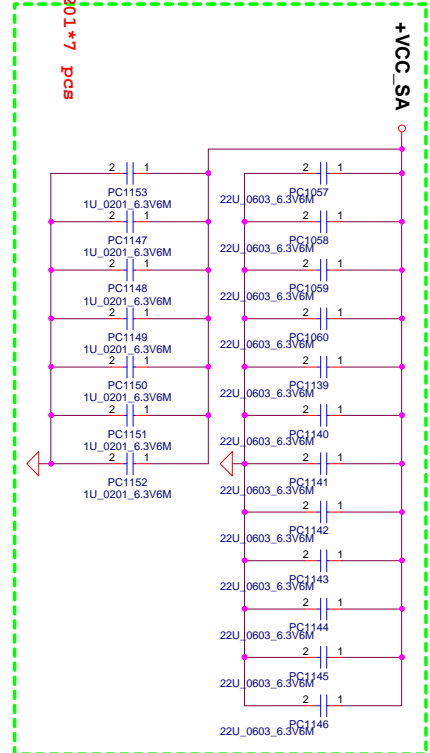
Size Document Number LA-E082P Rev 0.1  
Date: Monday, December 12, 2016 Sheet 83 of 71



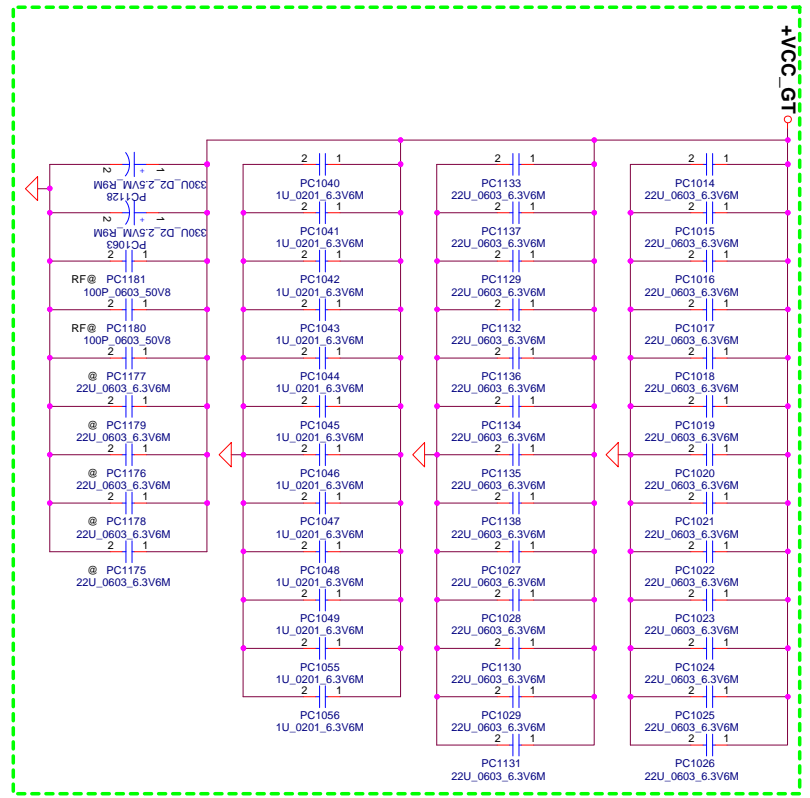
VCC CORE Place on CPU  
22U\_0603 \* 33 pcs +1U\_0201\*35 pcs  
+330U\_D2\*2 pcs



VCC SA Place on CPU  
22U\_0603 \* 12 pcs + 1U\_0201\*7 pcs



VCC GT Place on CPU (U22)  
22U\_0603 \* 26 pcs +1U\_0201\*12 pcs  
+330U\_D2\*2 pcs



**vinafix**

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**PROCESSOR DECOUPLING**

Document Number **LA-E092P**

Rev 0.1

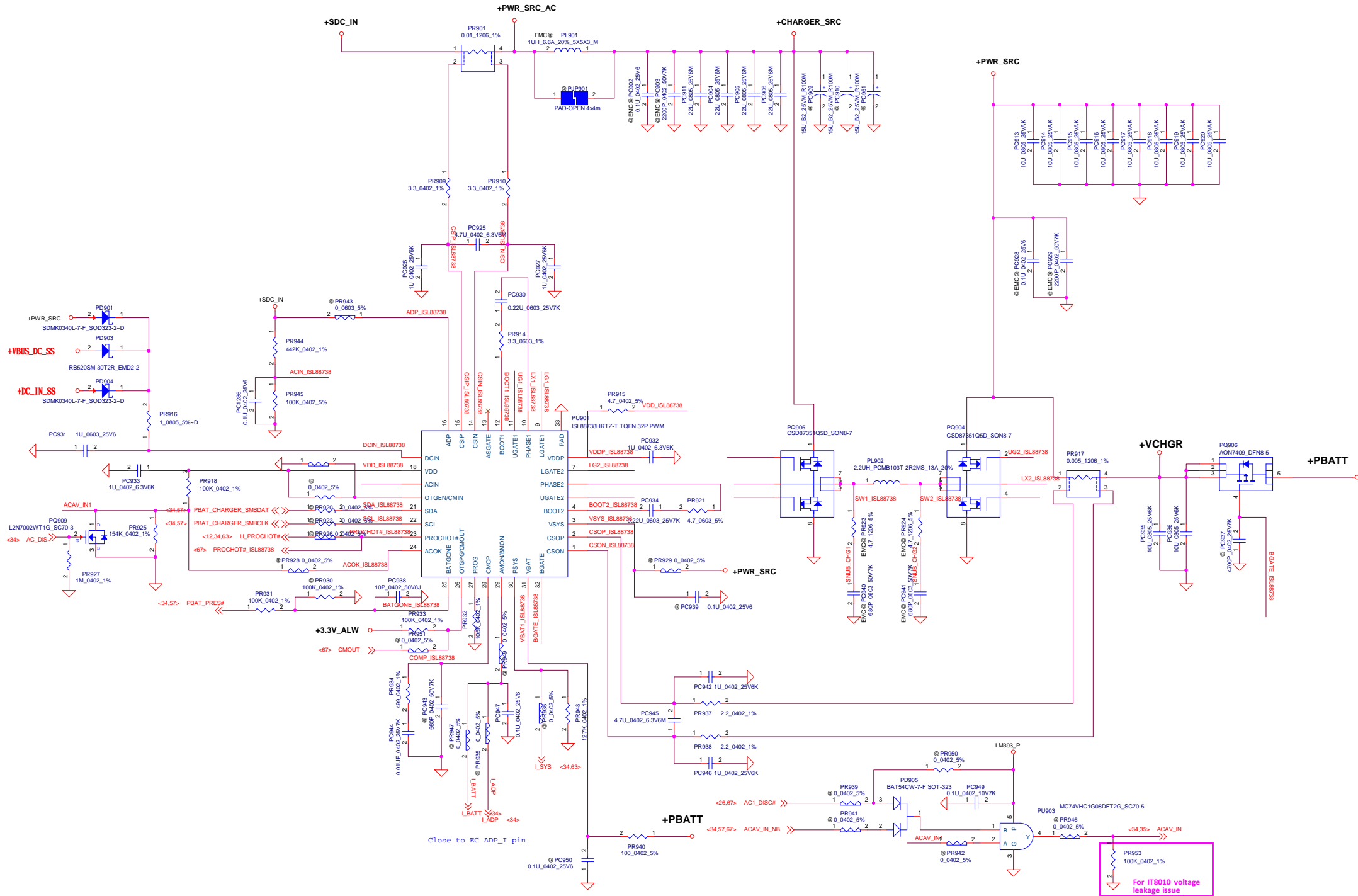
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Size

Date

Sheet 65 of 71

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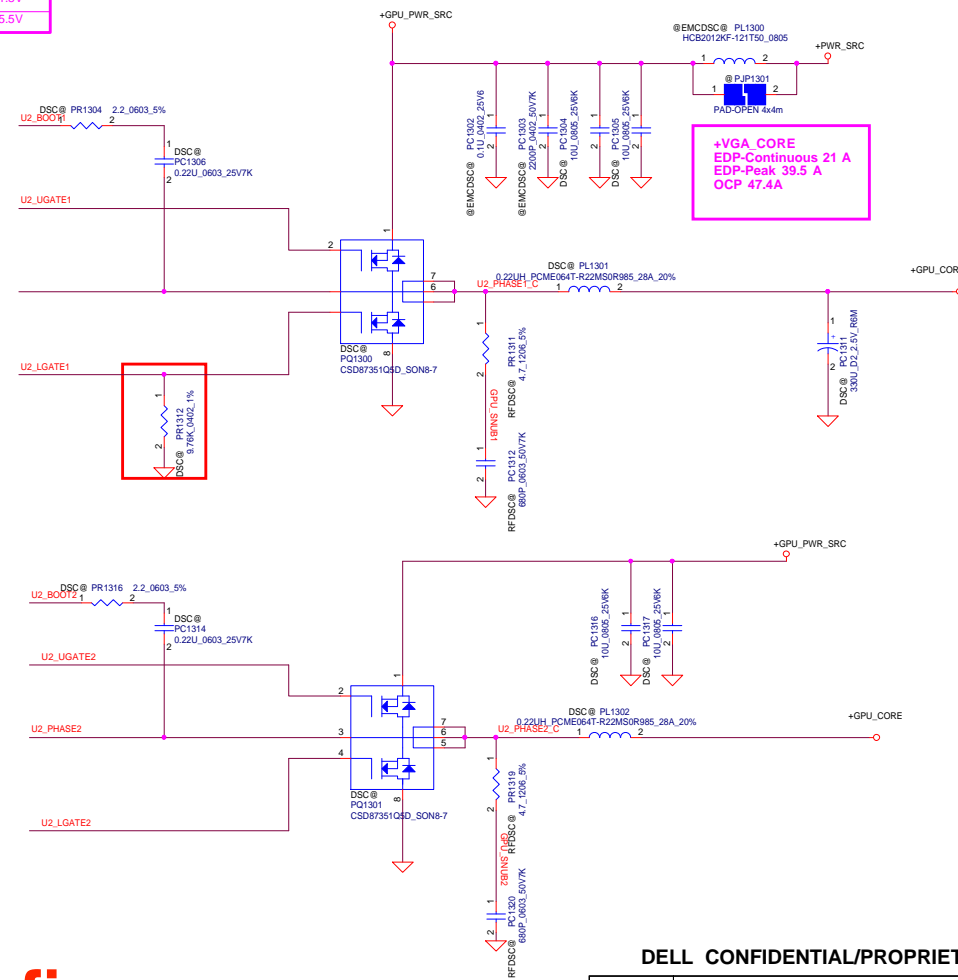


$$V_{step} = (V_{max} - V_{min}) / N_{max}$$

OCP=47.4A/2=23.7A per phase  
I<sub>valley</sub>=23.7A-12.12A/2=17.64A

$$C = 1 \times 330 \mu\text{F} \text{ (6mohm)} = 330 \mu\text{F}$$
$$V_{\text{ripple}} = I_{\text{ripple}} \times \text{ESR}(\text{min}) = 12.79 \text{A} \times 6 \text{mohm} = 76.74 \text{mV}$$

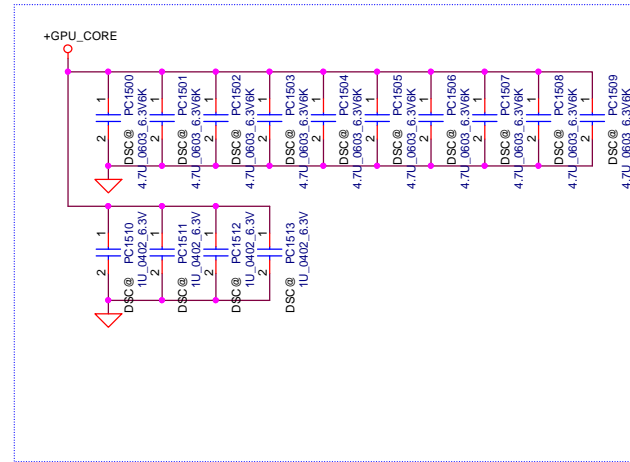
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

[illegible]

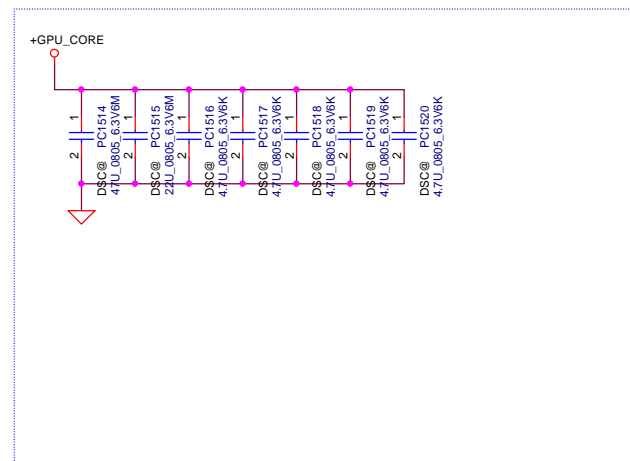
Rev	0.1
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nVidia GB4-64 package  
Under GPU  
4.7uF 0603 \* 10  
1uF 0402 \* 4



nVidia GB4-64 package  
Near GPU  
47uF 0805 \* 1  
22uF 0805 \* 1  
4.7uF 0805 \* 5

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Title			
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Size	Document Number	Rev	
	LA-E082P	0.1	
Date:	Monday, December 12, 2016	Sheet	70 of 71

# Version Change List ( P. I. R. List )

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	67	1Type-C PD Selector	2016 05/20	Compal	Change the S4 fast turn off circuit to avoid the leakage.	Re-connect the PR1251.1 and PQ1215.3 from +VBUS_DC_SS to +AC_IN.	X01
2	66	CHARGER	2016 05/30	Compal	Add the Circuit for Multiple Input Detach detection & PROCHOT#	Add PR960 0_0402_5%(SD028000080) and depop PR919 0_0402_5%(SD028000080) let the PU901.20 CMIN connect to GND. PU901.23 add cross page net PROCHOT#_ISL88738	X01
3	67	1Type-C PD Selector	2016 05/30	Compal	Add the Circuit for Multiple Input Detach detection & PROCHOT#	Add PQ1216 DMN65D8LW-7_SOT323-3(SB00000U000) to drive the PROCHOT# Reserve PC1217 1500P_0402_50V7K(SE074152K80)	X01
4	67	1Type-C PD Selector	2016 06/13	Compal	For Temp/Voltage test to fine tune the DC-IN detect voltage from 17.6V to 16.9V	PR1219 change from 22.6K to 23.2K(SD034232280)	X01
5	63~64	VCCSA_ISL95857 VCC_CORE/ GT_ISL95857	2016 06/13	Compal	location alignment	IA_CORE change location PU603 to PU610, PL603 to PL610 GT_CORE change location PU604 to PU612, PL604 to PL612 SA_CORE change location PU606 to PU614, PL601 to PL614	X01
6	66	CHARGER	2016 06/13	Compal	To decrease the charger input leakage voltage for TypeC AC.	PD903 change from SDMK0340L-7-F_SOD323-2~D(SCS0340L010) to RB520SM-30T2R_EMD2-2(SCS00006C00)	X01
7	57 67	+DCIN 1Type-C PD Selector	2016 06/20	Compal	To solve the MOS leakage problem to avoid the error active.	PR12, PR11, PR1205, PR1207, PR1228 change from 1M_0402_5%(SD028100480) to 499K_0402_1%(SD034499380) PR16, PR18, PR1212, PR1213, PR1229 change from 1M_0402_5%(SD028100480) to 49.9K_0402_1%(SD034499280) PR10, PR1251 and PR1202 change from 100K_0402_5%(SD028100380) to 300K_0402_1%(SD034300380)	X01
8	63	VCCSA_ISL95857	2016 06/22	Compal	IA/GT/SA CORE static LL optimization	PC621, PC647 change from 680P(SE074681K80) to 1200P(SE074122K80) PR640 change from 383_0402_1%(SD034383080) to 365_0402_1%(SD034365080) PR638 change from 374_0402_1%(SD034374080) to 340_0402_1%(SD00000KT80) PR629 change from 93.1K_0402_1%(SD034931280) to 95.3K_0402_1% (SD034953280)	X01
9	66	CHARGER	2016 06/27	Compal	EMI request	PR921 change from 2.2_0603_5%(SD013220B80) to 4.7_0603_5%(SD013470B80) PR914 change from 0_0603_5%(SD013000080) to 3.3_0603_1%(SD014330B80) pop PR923, PR924 4.7_1206_5%(SD001470B80) pop PC940, PC941 680P_0603_50V7K(SE025681K80)	X01
10	58~61 68~69	+5V/+3.3V +1.2V_MEN +0.6V_DDR 1VALWP/VCCIO PRIM GPU_COREP/GPU_VRAM	2016 06/28	Compal	RF request	pop PC100, PC103, PC115, PC116, PC301, PC303, PC409, PC1400, PC1402 100P_0402_50V8J(SE071101J80) pop PC1320, PC1312, PC204, PC302, PC112 680P_0603_50V7K(SE025681K80) pop PR1319, PR1311, PR202, PR303, PR106 4.7_1206_5%(SD000010280)	X01
11	66	CHARGER	2016 07/01	Compal	Reserve the OVP function to protect the typeC device.	Depop PJF1202, PR1255, PR1239, PR1246, PC1211, PR1237, PC1212 , PD1205, PC1213, PC1214, PR1248 Change PR1247 from 200K_0402_1%(SD034200380) to 100K_0402_1%(SD034100380) Re-modify the S11 OVP description to S3 OVP.	X01
12	66	CHARGER	2016 07/01	Compal	Change the charger version from A version to B version.	Change PU901 from ISL88738HRTZ REV.A-T TQFN 32P PWM(SA00009VW10) to ISL88738HRTZ REV.B-T TQFN 32P PWM(SA00009VW20)	X01
13	66	CHARGER	2016 09/02	Compal	For IT8010 voltage leakage issue	Add PR953 100K_0402_1%(SD034100380)	X03
14	63	+VCCSA_ISL95857	2016 09/21	Compal	Change CPU core version to MP version.	Change PU602 from SA0000A4A00 to SA0000A4A0L	X03
15	61	VCCIO/PRIM	2016 09/29	Compal	PCH LPM function	Unpop PR410 0_0402_5%(SD028000080) Pop PR426 0_0402_5%(SD028000080)	

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Title			
P.I.R			
Size	Document Number	Rev	
	LA-E082P	01	
Date:	Monday, December 12, 2016	Sheet	71 of 71

# Version Change List ( P. I. R. List )

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	HW	2016/05/24	COMPAL	For Schematic align	Remove RA2	0.2(X01)
2	35	HW	2016/05/24	COMPAL	Symbol pin name change	UE1.C1 pin name change to GPIO024/nRESETI	0.2(X01)
3	9	HW	2016/05/24	COMPAL	Symbol pin name change	UT5.A6/A7/A8/B7 pin name change to GND, UT5.D6 pin name change to HRESET	0.2(X01)
4	25	HW	2016/05/24	COMPAL	Symbol pin name change	UT9.20 pin name change to SNK_CAD/DCI_DAT, UT9.32 pin name change to HPDIN/DCI_CLK	0.2(X01)
5	6	HW	2016/05/24	COMPAL	DP HPD base on INTEL PDG	Delete RC312/RC242	0.2(X01)
6	25	HW	2016/05/24	COMPAL	Disable AUX snoop feature	Pop RT308	0.2(X01)
7	33,40	HW	2016/05/24	COMPAL	Remove HDD LED MUX feature	Depop RN100/RN101	0.2(X01)
8	35	HW	2016/05/24	COMPAL	PORT80_DET#	Reserve RE513 100k (SD028100380) to GND	0.2(X01)
9	6	HW	2016/05/24	COMPAL	Follow Intel PDG AUX topology	Delete RC179/RC180/RC181/RC182 Add test point T281/T282 for CPU_DP1_AUXN and CPU_DP1_AUXP	0.2(X01)
10	17	HW	2016/05/24	COMPAL	S0ix(modern standby) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
11	46						0.2(X01)
12	43,46					1.add CLIP1	0.2(X01)
13	25	HW	2016/05/27	COMPAL	For Schematic align	SW2_DP1_HPDP Add RT380 place near TUSB546	0.2(X01)
14	30	HW	2016/06/01	INTEL	Intel reviwie result	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(@)_0201 to 10uF_0603 CZ32/CZ31/CZ29 place near JNGFF1.2/JNGFF1.4 CZ27/CZ30/CZ28 place near JNGFF1.72/JNGFF1.74	0.2(X01)
15	37,38	HW	2016/06/07	DELL	change to Nuvoton TPM form ATMEL TPM	Delete ATMEL TPM circuit, Add Nuvoton TPM circuit	0.2(X01)
16	12	HW	2016/06/07	INTEL	Intel MOW request	Add CC331 2.2PF (SE07122AC80) for HDA_RST# Add CC332 2.2PF (SE07122AC80) for HDA_SDIN0 Add CC333 2.2PF (SE07122AC80) for HDA_SDOUT	0.2(X01)
17	33	HW	2016/06/07	INTEL	Intel reviwie result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
18	33	HW	2016/06/07	COMPAL	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
19	35	HW	2016/06/07	COMPAL	For MEC5105K-D1-TN sample	1.UE1 change to SA00009GL00(S IC MEC5105K-D1-TN WFBGA 169P EC) 2.Depop RE361,Pop RE360,RE362	0.2(X01)
20	46	HW	2016/06/17	COMPAL	Base on ME drawing	H10 change from H_4P0 to H_3P0	0.2(X01)

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Compal Electronics, Inc.			
Title EE P.I.R (1/6)			
Size	Document Number	Rev	
	LA-E082P	1.0	
Date:	Monday, December 12, 2016		
Sheet	72	of	75

# Version Change List ( P. I. R. List )

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
21	42	HW	2016/06/17	COMPAL	Base on USB3 EA result,B_EQ change to13dB	Depop RI42,pop RI44	0.2(X01)
22	11	HW	2016/06/17	COMPAL	Base on Crystal EA result	CC23 change form 15pF to 12pF	0.2(X01)
23	41	HW	2016/06/17	COMPAL	BITS284924-HDD is still working after press power button into S5 during POST.	Depop RN5	0.2(X01)
24	38,45	HW	2016/06/20	COMPAL	ME request	1.JKBTP1 change from HRS_TF49-20S-0P5SH_20P-T to CVILU_CF5020FD0RK-05-NH_20P-T 2.JUSH1 change from HRS_TF49-26S-0P5SH_26P-T to CVILU_CF5026FD0RK-05-NH_26P-T	0.2(X01)
25	34	HW	2016/06/20	COMPAL	Base on Audio EA result	RA7,RA8 change from 24.9 to 16.2 ohm(SD00001U900)	0.2(X01)
26	30	HW	2016/06/22	COMPAL	EMI request	CL22 change from 1500pF to 10pF (SE167100J80 S CER CAP 10P 3KV J NPO 1808 AC250V X2Y3)	0.2(X01)
27	29	HW	2016/06/22	COMPAL	EMI request	Change LV1 from SM01000BV00 to SM01000NY00	0.2(X01)
28	29	HW	2016/06/22	COMPAL	ME request	JIR1 change from SP010023D00 to SP010013W20	0.2(X01)
29	35	HW	2016/06/22	DELL	The possibility of GPIO map update,RTCRST_ON change from GPIO141 to GPIO122	Add RE514(@),RE515 for RTCRST_ON	0.2(X01)
30	36						0.2(X01)
31	29	HW	2016/06/22	COMPAL	RF request	CA7 CZ1 change to 100pF(0201)SE174101J80	0.2(X01)
32	12	HW	2016/06/22	COMPAL	BIOS need detect Storage type and dynamic change the name	UE1.D7 add HDD_DET#	0.2(X01)
33	24	HW	2016/06/28	COMPAL	For VGA test result	Pop RV121/RV122/CV132/CV133	0.2(X01)
34	46	HW	2016/06/28	COMPAL	For DFX request	CLIP1.1 change from GND to NC	0.2(X01)
35	38	HW	2016/06/29	COMPAL	X8 have no difference JUSH1 pin define concern	Depop DZ7,Pop RZ87	0.2(X01)
36	38	HW	2016/06/29	COMPAL	Let USH_PWR_STATE# keep low at S5	RZ10 change from 1M to 100k ohm	0.2(X01)
37	36	HW	2016/06/29	COMPAL	Foe X01 Board ID	RE79 change from 240k to 130k ohm	0.2(X01)
38	41	HW	2016/06/29	COMPAL	BITS283552 - [BR_CSLP] FFS AP no function when execute FF generator or shake SU	FFS VDD_IO change to +3.3V_RUN	0.2(X01)
39	29	HW	2016/08/04	COMPAL	RF request	POP CC27 & change value from 22p to 47p	0.3(X02)
39	18	HW	2016/08/04	COMPAL	DSC BOM change	Pop RC385, Depop RC386	0.3(X02)

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DELL CONFIDENTIAL/PROPRIETARY			
Compal Electronics, Inc.			
Title EE P.I.R (2/6)			
Size	Document Number	Rev 1.0	
Date: Monday, December 12, 2016		Sheet 73	of 75

# Version Change List ( P. I. R. List )

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40	34, 35	HW	2016/08/04	COMPAL	Vendor schematic review	1. Add net WRST# to UE2.4 and CE500 luf (SE000000K80) 2. Add RE523 0 ohm for UE2 power pin soft start 3. Change RE14,RE15,RE18 from 100k ohm to 10k ohm 4. Change RPE12.1 to RE524 (10Kohm) for EXPANDER_GPU_SMDAT 5. Change RPE12.2 to RE525 (10Kohm) for EXPANDER_GPU_SMCLK 6. Reserve CE504-CE505 for EXPANDER_GPU_SMDAT/CLK to GND.	0.3(X02)
41	14	HW	2016/08/04	COMPAL	Intel suggestion	RC137 change from 1K to 3K	0.3(X02)
42	27	HW	2016/08/04	COMPAL	For UT7 2nd source issue	Add RT393 PD 100K ohm to +5V_PD_VDD for discharging instantly	0.3(X02)
43	45	HW	2016/08/04	COMPAL	Touchpad I2C EA	Chagne RZ20, RZ21 from 4.7k ohm to 2.2k ohm Change CZ80, CZ81 from 330pf to 10pf	0.3(X02)
44	26	HW	2016/08/04	COMPAL	For PD sample	Change UT5 from SA00009W200 to SA00009W210	0.3(X02)
45	42	HW	2016/08/05	COMPAL	BITS290368-System can't be waked from S3 when connect to right USB port via USB3.0 to LAN Dongle.	USB3 repeater power rail Add RI79 0ohm to +3.3V_RUN and De-pop it. Add RI80 0ohm to +3.3V_ALW_PCH and pop it.	0.3(X02)
46	11	HW	2016/08/08	COMPAL	EMI request	add RC417 (0 ohm) for Xtak24_IN	0.3(X02)
47	42	HW	2016/08/08	COMPAL	schematic modify	1. pop RI37 2. RI79, RI80 footprint change form 0402 to 0603 3. add QI1 controlling USB3 repeater PD#	0.3(X02)
48	32, 37	HW	2016/08/09	COMPAL	DFB request	SMT concern DZ1, DZ2, DZ5, DZ6 PCB pad is too small, suggest use the symbol "RB520SM-30T2R_EMD2-2" follow PD903	0.3(X02)
49	18						0.3(X02)
50	48						0.3(X02)
51	33, 35, 48	HW	2016/08/10	COMPAL	Footprint align	DA8,DE1,DV10 follow symbol "RB520SM-30T2R_EMD2-2"	0.3(X02)
52	42	HW	2016/08/11	COMPAL	schematic modify	change USB repeater PD# enable pin to "USB_PWR_SHR_VBUS_EN"	0.3(X02)
53	35	HW	2016/08/11	COMPAL	schematic align	add power rail +3.3V_ALW_UE2 for UE2	0.3(X02)
54	42	HW	2016/08/12	COMPAL	schematic modify	delete QI1, depop RI37, add RI81 connecting "USB_PWR_SHR_VBUS_EN" & "USB3_PD#"	0.3(X02)
55	42	HW	2016/08/16	COMPAL	EA request	depop RI38, RI44, RI53, RI57 for USB3 repeater	0.3(X02)
56	9	HW	2016/09/08	COMPAL	DGPU_PWR_EN need to use BIOS solution	depop RC385,pop RC386	0.4(X03)
57	38	HW	2016/09/08	COMPAL	TPM change to NPCT650VB2YX	Change UZ12 from to SA00008EL70 to SA00008EL80	0.4(X03)
58	35	HW	2016/09/08	COMPAL	Expander I/O change from ITE8010 to MCP23008	Change UE2 from SA00009VL00 to SA0000ADQ00, remove RE523 Change RE524, RE525 from 10Kohm to 2.2Kohm	0.4(X03)
59	34	HW	2016/09/08	COMPAL	Board ID	Change RE79 to 33kohm (SD028330280)	0.4(X03)
60	34	HW	2016/09/08	COMPAL	schematic align	Reserve RE526(10K) PU for USH_DET# to +3.3V_ALW	0.4(X03)
61	34	HW	2016/09/08	COMPAL	EC request for power consumption	Add RE505 PU to +3.3V_ALW for LOM_CABLE_DETECT# (Reserve) Add RE532 PU to +3.3V_ALW for BCM5882_ALERT#	0.4(X03)
62	37	HW	2016/09/08	COMPAL	USH/B de-pop, pop on MB side	POP RZ8,RZ9 for USH SMBus	0.4(X03)
63	35	HW	2016/09/20	COMPAL	DELL request	Add RE536/RE537 for resistors for PCH_DPWROK circuit	0.4(X03)
64	34	HW	2016/09/20	COMPAL	WDT schematic option 2	use Option2: pop RE361 / depop RE362	0.4(X03)
65	33	HW	2016/09/20	COMPAL	EMI request	1. L6~L9 change to 80ohm bead (BLM15PD800SN1D, SM01000N000) for BR14/15 2. depop CA2, CA3 3. RA55,RA56 change location toLA15, LA16 with 33ohm bead (BLM15PX330SN1D,SM01000NA00)	0.4(X03)
66	39	HW	2016/09/20	COMPAL	NV GPU sequest	CV247 change from 3900pf to 4700pf (SE075472K80) CV248 change form 220pf to 470pf (SE074471K80)	0.4(X03)
67	35	HW	2016/09/20	COMPAL	EMI request	RC295/RC417 change from 0 to 33 ohm	DELL CONFIDENTIAL/PROPRIETARY

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<b>EE P.I.R (2/6)</b>		
Size	Document Number	Rev 1.0
<b>LA-E082P</b>		
Date: Monday, December 12, 2016		
Sheet 74 of 75		

Version Change List ( P. I. R. List )

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
68	35	HW	2016/10/04	COMPAL	BITS294007 - Sometimes need to press power button twice to power on system.	CE12 change to 2.2u (SE000008880) RE33 change to 1K (SD028100180)	0.4(X03)
69	24	HW	2016/10/04	COMPAL	U-line VGA EA PASS	depop RV121/RV122	0.4(X03)
70	26	HW	2016/10/04	COMPAL	TI CC pin for ESD request	CT85,CT86 change to 470p.(SE074471k80)	0.4(X03)
71	25	HW	2016/10/04	COMPAL	BR14 OTP issue	RE77 change to 1.69K_1% (SD00000JB80)	0.4(X03)
72	35	HW	2016/10/04	COMPAL	EC watchdog reserve	add QE13,RE530,CE503	0.5(X04)
73	34	HW	2016/10/06	COMPAL	UE1.H8 to prevent EOS issue on MEC5105	Add RE539(100ohm) to CV2_ON	0.5(X04)
74	36	HW	2016/10/06	COMPAL	BOARD ID	Change RE79 to 8.2k ohm(SD028820180)	0.5(X04)
75	36	HW	2016/10/31	COMPAL	BOARD ID	Change RE79 to 4.3k ohm(SD028430180)	1.0(A00)
76	36	HW	2016/10/31	COMPAL	Change R1 to R3 for MP part	Change UL1 CP/N to SA000081G1L Change UE1 CP/N to SA00009GL30 change UV1 CP/N to SA00009S01L	1.0(A00)
77	36	HW	2016/10/31	COMPAL	For DFB request.	Close solder mask CMOS1 (-NPM) and other co-lay part	1.0(A00)
78	36	HW	2016/10/31	COMPAL	Service Mode Switch remove	Depop SW1 and RC222 and RC221 change to short pad	1.0(A00)
79	36	HW	2016/10/31	COMPAL	RE374 change BS to LPC@	RE374 change BS to LPC@	1.0(A00)
80	36	HW	2016/10/31	COMPAL	For MEC5105 rev. C	Pop RE362,RE536; Depop RE361,QE13,CE503,RE530,UE7,CE5,CE6,RE348,RE537	1.0(A00)
81	36					IGS	1.0(A00)

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EE P.I.R (2/6)

Size

Document Number

LA-E082P

Date: Wednesday, December 14, 2016

Sheet 75 of 75

Rev 1.0